Nanoelectronics

Lecture 9

Emerging (non-volatile) memories:

- Phase Change Memory (PCM)
- RRAM
- Magnetic memory: Spin Transfer Torque RAM (STTRAM)
- Ferroelectric RAM

Prof. Adrian M. Ionescu, presented by Dr. I. Stolichnov

Optional reading on emerging memories: reviews

Progress of emerging non-volatile memory technologies in industry

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MRS Communications

Overview and outlook of emerging non-volatile memories

Mengwei Si, Huai-Yu Cheng, Takashi Ando, Guohan Hu, and Peide D. Ye*

Memory technologies with higher density, higher bandwidth, lower power consumption, higher speed, and lower cost are in high demand in the current big data era. In this paper, recent progress of emerging non-volatile memories is reviewed. The current status, challenges, and opportunities of emerging non-volatile memories, such as phase-change memory, resistive random-access memory, ferroelectric field-effect transistors, and magnetic random-access memory, are discussed toward storage-class memory, embedded non-volatile memories, and near/in-memory computing applications.

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Key questions

- Quest for universal memory: no single universal memory now, for what purpose?
- Who are today's memory candidates for tomorrow applications?
- What physical mechanisms to store the information in a non-volatile memory cell?
- Challenges, limitations, comparison with existing memories adopted by industry

Outline

- Memories: **importance and categories**

- **State-of-the-art and emerging memories – towards an universal memory ultra-dense and ultra-fast. Main question: are current memories scalable, reliable and energy efficient enough?**

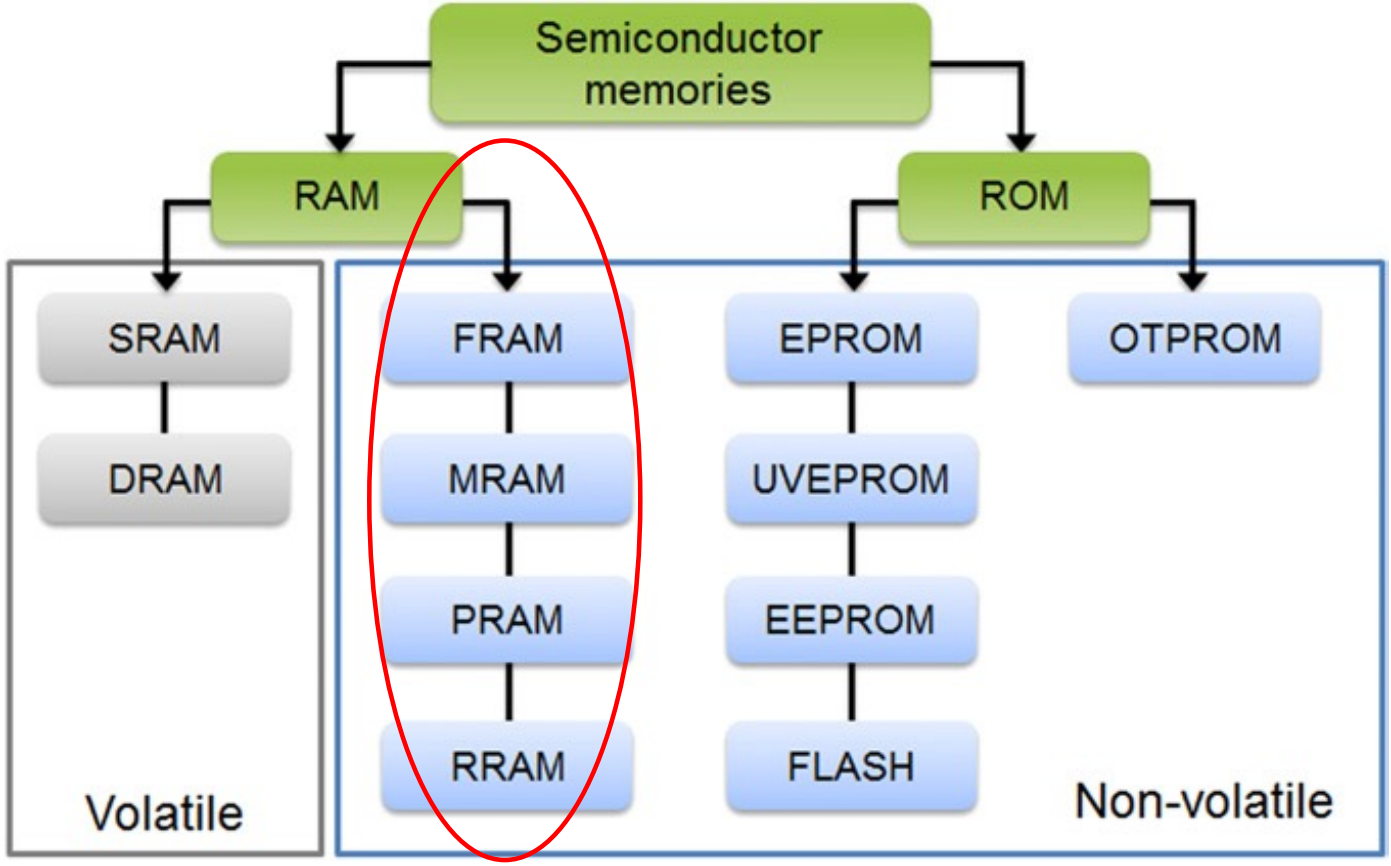
- **Main candidates considered by industry:**
  - **Phase Change Memories (PCM)**
  - **Resistive RAM (RRAM)**
  - **Magnetic: Spin Transfer Torque RAM (STTRAM)**
  - **Ferroelectric memories (FRAM)**

Memory categories (1)

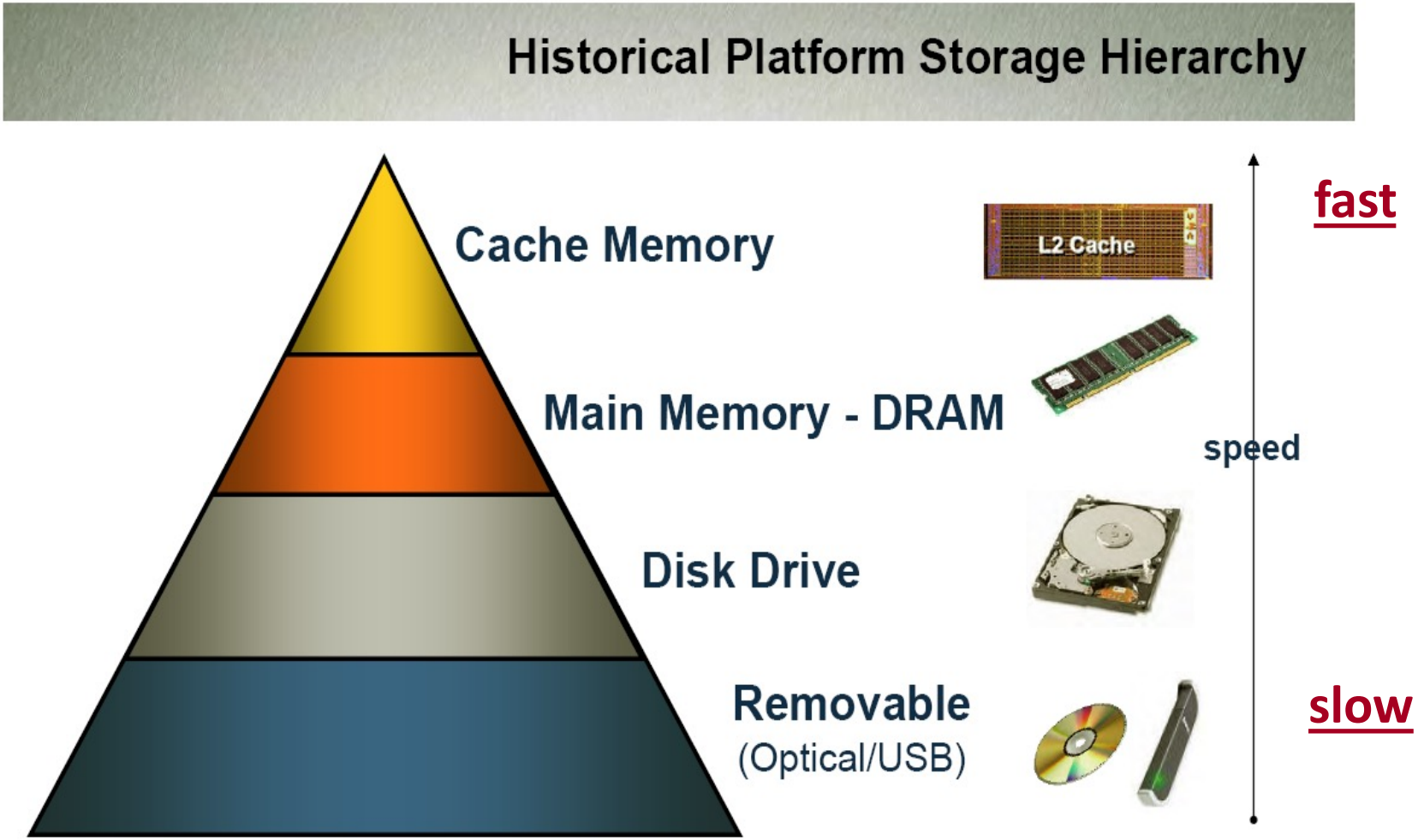
- Semiconductor memories are classified based on how many times they can be rewritten:
  - **Random Access Memories (RAMs)** -- information can be written to or read from any cells without read/write cycle limitations. Writing and reading times are almost the same
  - **Read-Only Memories (ROMs)** - read/write cycles are limited. Re-writing is in many cases possible but takes more time than reading.
  - ROMs are nonvolatile, that is, the stored information remains even if the power is turned off.

Memory categories (2)

- Volatile and non-volatile

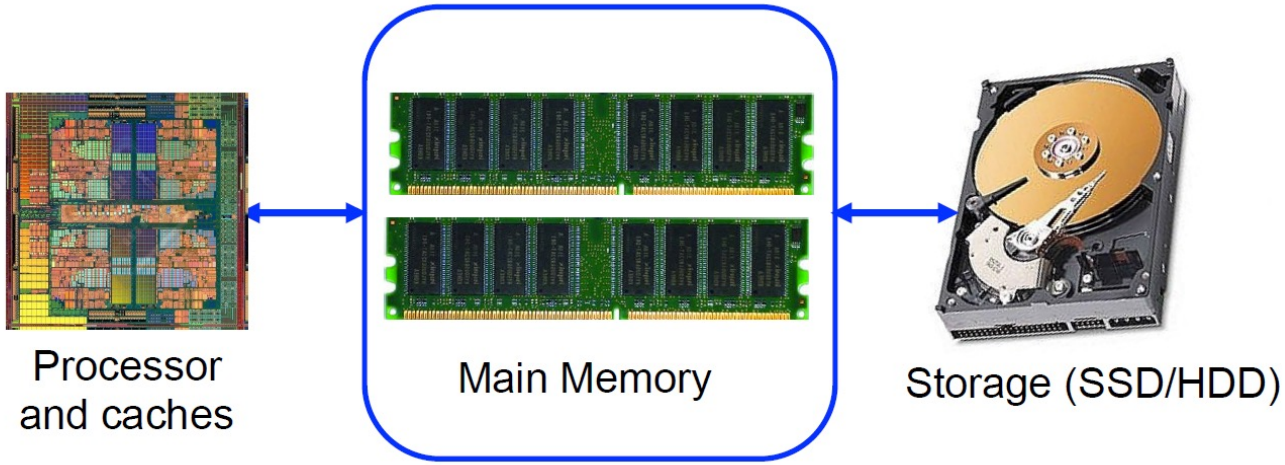


Memory hierarchy



SRAM and DRAM

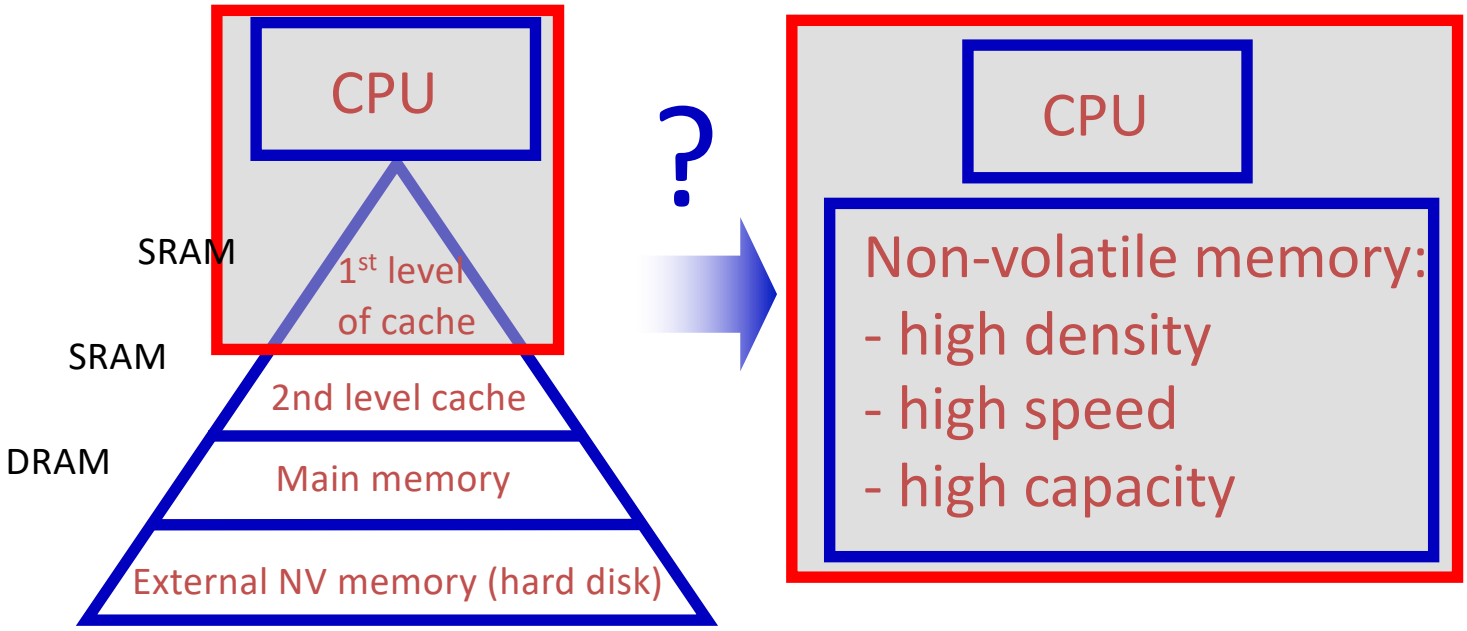
- **SRAMs are very fast** (write/erase time: 0.3 ns/0.3 ns) compared with DRAMs (write/erase time: <10 ns/<10 ns), **but their density is very low due to the large unit cell size** (six transistors in latched configuration with a minimum cell size of 140F2, where F is the minimum feature size) compared with DRAMs, the unit cell of which is much smaller (one-transistor and one-capacitor (1T1C) stack with a minimum cell size of 6F2).
- **SRAMs are used as cache memories** where the access time is critical, while **DRAMs are used as main memories** where the capacity is critical for temporary information storage and processing.



Quest for universal memory

New electrically accessible **non-volatile memory with high speed and high density** would imply a revolution in computer architectures (avoid slow non-volatile external storage medias):

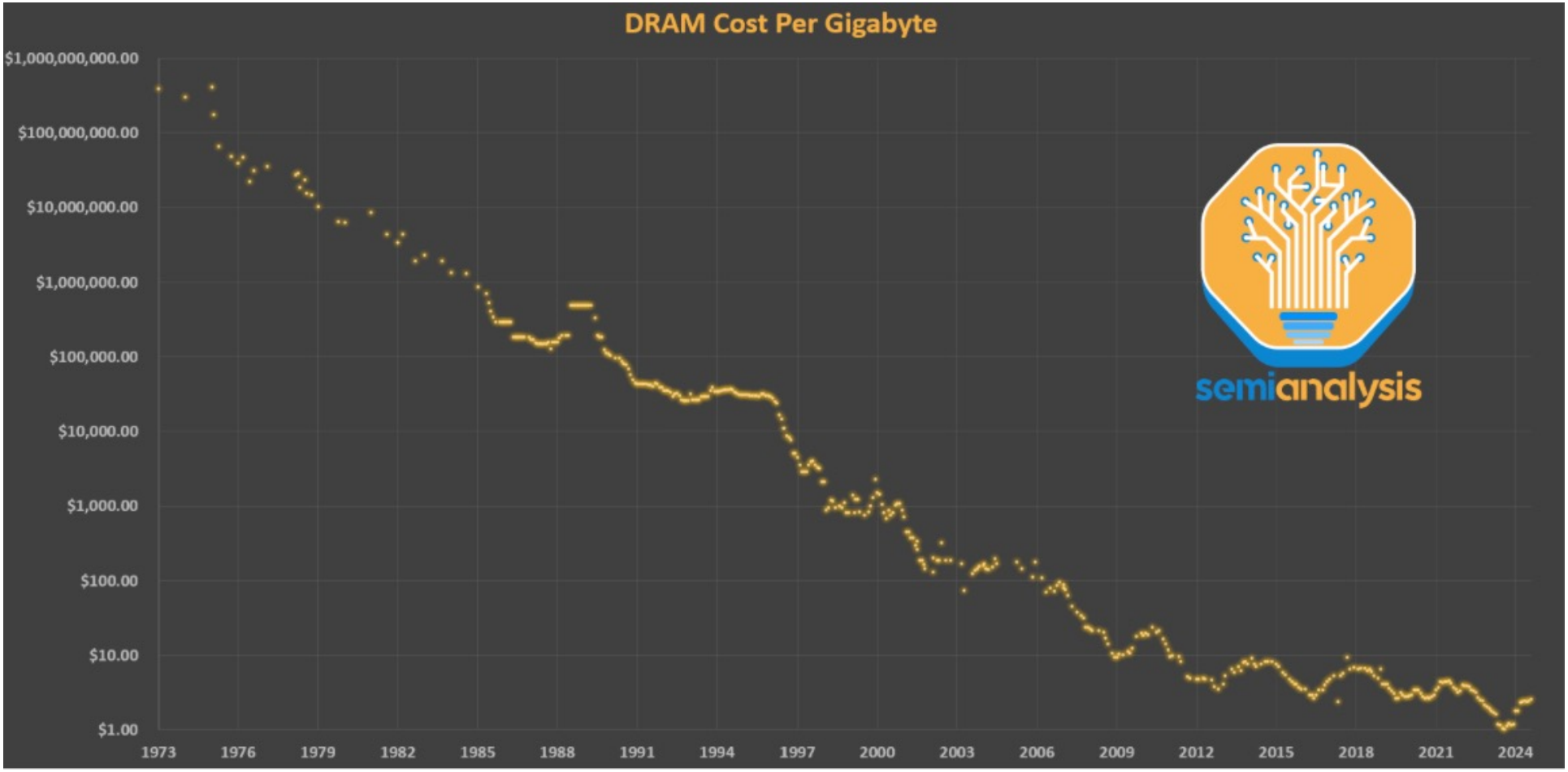
new memory hierarchy



Major trends affecting the main memory

- Need for main memory capacity and bandwidth increasing
- Main memory energy/power is a key system design concern
- DRAM technology scaling is ending
- DRAM does not scale easily below 35 nm
- Scaling has provided many benefits:
  - higher capacity, higher density, lower cost, lower energy
- **What solutions? Emerging non-volatile memories?**

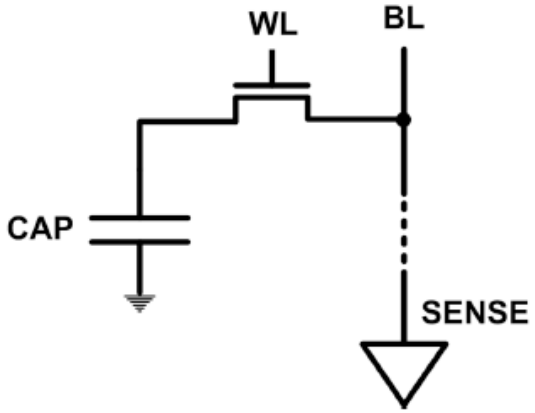
DRAM cost per Gigabyte

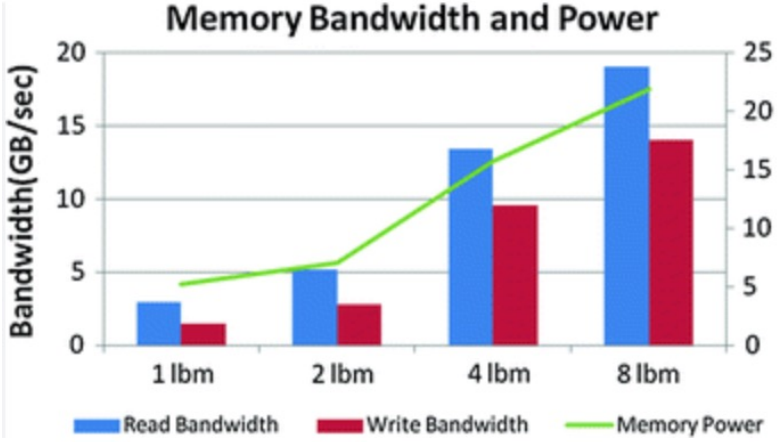


Classical DRAM scaling is economically and energetically saturated

DRAM is a reference, however is has limitations: scaling problem, energy consumption, volatility

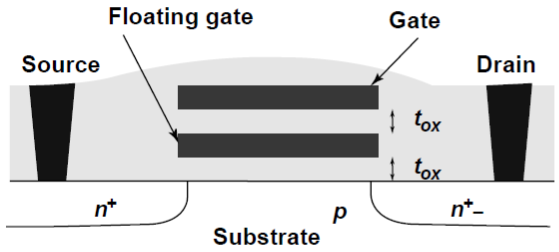
- **DRAM stores charge in a capacitor (charge-based memory)**
  - Capacitor must be large enough for reliable sensing
  - Access transistor should be large enough for low leakage and high retention time
  - Scaling beyond 35nm **IRDS** (Industry Roadmap for Devices and Systems)
  - By its principle, **DRAM capacity, cost, and energy/power hard to scale**

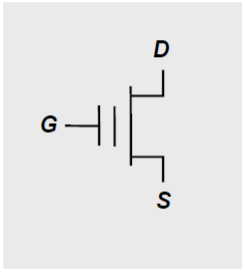


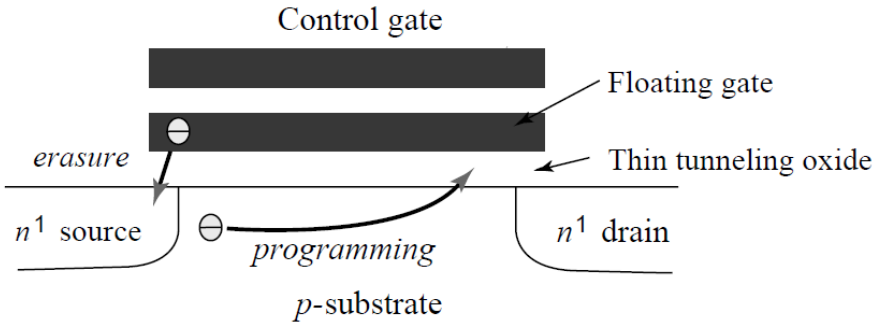


Mainstream nonvolatile memory – FLASH, some history

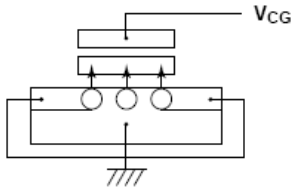
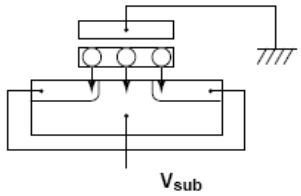
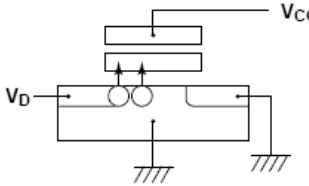
Flash memory: invented by Fujio Masuoka while working for Toshiba in 1984. According to Toshiba, the name 'Flash' was suggested by Dr. Masuoka's colleague, Mr. Shoji Ariizumi, because the erasure process of the memory contents reminded him of a flash of a camera. Dr. Masuoka presented the invention at the IEEE 1984 Integrated Electronics Devices Meeting held in San Jose, California. Intel saw the massive potential of the invention and introduced the first commercial NOR type flash chip in 1988.

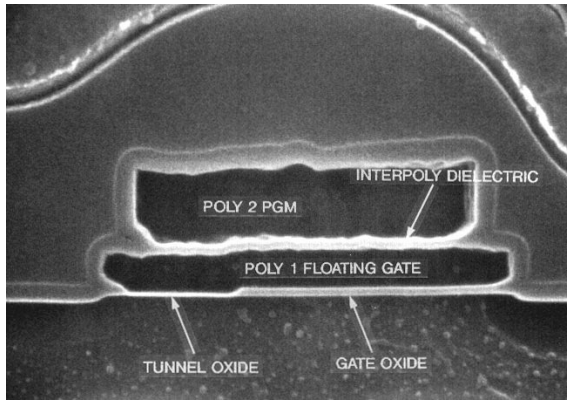






FLASH operation

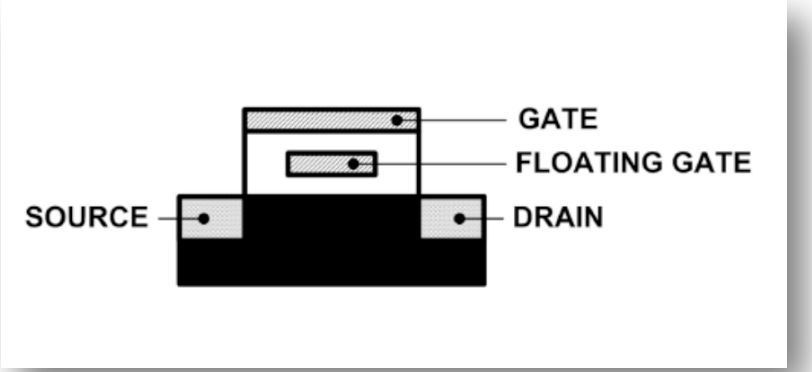
	Electron Trapping	Electron Removal
Bi-polarity FN-t Write / Erase technology	 Fowler-Nordheim tunneling	 Fowler-Nordheim tunneling
Hot-Electron injection and FN-t technology	 Hot-Electron Injection	



- **Electrons are injected and trapped onto the floating gate**. Electrons are trapped in the floating gate following Fowler-Nordheim tunneling or hot electron injection
- These **electrons modify the threshold voltage** of the storage transistor..
- **Electrons are removed from the floating gate** using Fowler-Nordheim tunneling

Limitations in FLASH memory

- FLASH memory is a class of EEPROM
- Each memory cell in a FLASH memory consists of only one metal–oxide–semiconductor field-effect-transistor (MOSFET) with an additional floating gate, unlike EEPROMs(two MOSFETs).
- FLASH memories are much slower(write/erase time; 1 ms/0.1 ms) than DRAMs, and hence **they are used as secondary storage media**.
- FLASH memories (based on the Fowler–Nordheim tunnelling) will not reliably function at low voltages of 0.5V - 1V) – typically V > 5V is needed
- FLASH memory technology has obvious disadvantages: long write and erase times as well as a **limited cyclability of $>10^5$ write/erase cycles compared with DRAM ($>3 \times 10^{16}$ write/read cycles) (see table)**



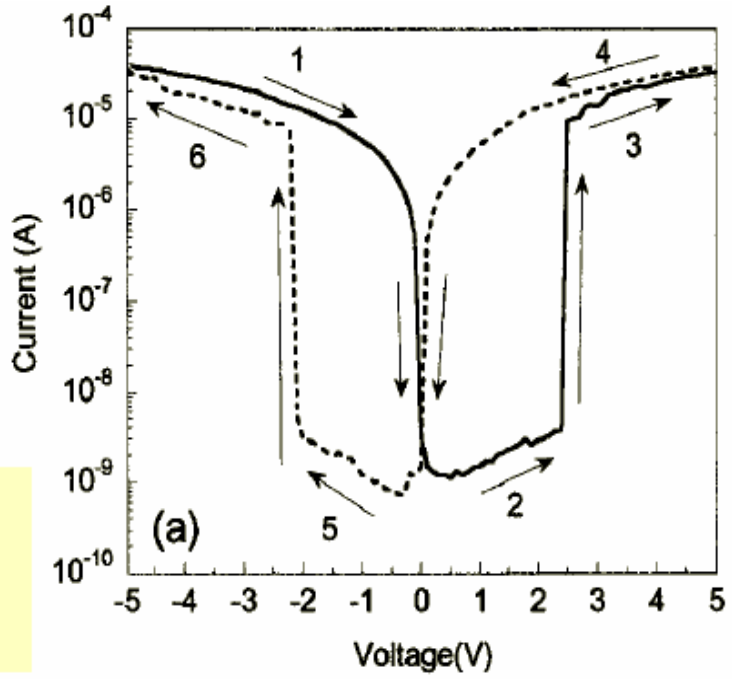
Development of new memory starts with memory materials

To make a memory, all you need is a hysteresis loop!

– Easy to find memory effect

– Difficult to satisfy memory requirements!

Example: Voltage bias induced resistance change (bi-directional programming)



- **The focus shifts from "replacing DRAM/FLASH" to compute-centric memory architectures**

Overview of state-of-the-art performance

Table 1. Comparison of conventional and emerging memories. Most data other than those of RRAMs were taken from [1]. RRAMs have not been demonstrated at the industrial level so some data, e.g. write/erase time and endurance, are of RRAMs at the laboratory level.

	Volatile memory		Non-volatile memory		Emerging non-volatile memory			
Type	SRAM	DRAM	NOR-FLASH	NAND-FLASH	MRAM	PRAM	FRAM	RRAM
Cell elements	6T	1T1C	1T	1T	1(2)T1R	1T1R or 1D1R[a]	1T1C	1T1R or 1D1R[a]
Cell	Latch	Stack/ trench capacitor	Floating gate/charge trap	Floating gate/charge trap	Magnetoresistance	Phase-change	Polarization-change	Resistance-change
Minimum cell size	$140F^2$	$6F^2$	$10F^2$	$5F^2$	$20F^2$	$4.8(4)F^{2b}$	$22F^2$	$4F^{2c}$
Write/erase time	0.3 ns/ 0.3 ns	<10 ns/ <10 ns	1 ms/ 10 ms	1 ms/ 0.1 ms	10 ns/ 10 ns	20 ns/ 50 ns	10 ns/ 10 ns	5 ns/5 ns [48]
Endurance (cycles)	$>3 \times 10^{16}$	$>3 \times 10^{16}$	$>10^5$	$>10^5$	$>3 \times 10^{16}$	10^8	10^{14}	$>10^{10}$ [49]
Application	Cache	Main memory	Storage	Storage	Storage	Storage	Storage	Storage/Main memory

[a] 1D1R (one-diode and one-resistor) unit cells are employed in passive PRAMs and RRAMs, which are based on crossbar-arrays.
[b] Passive crossbar-array-based PRAMs satisfy a minimum cell size of $4F^2$.
[c] Similar to passive PRAMs, passive RRAMs satisfy a minimum cell size of $4F^2$.

«Traditional»

Emerging (be careful with these numbers… will see details later…)

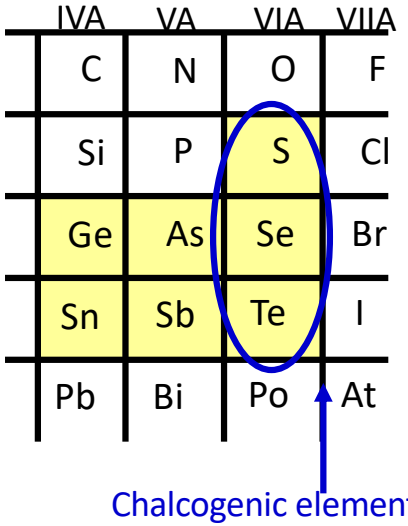
PHASE CHANGE MEMORY (PCM)

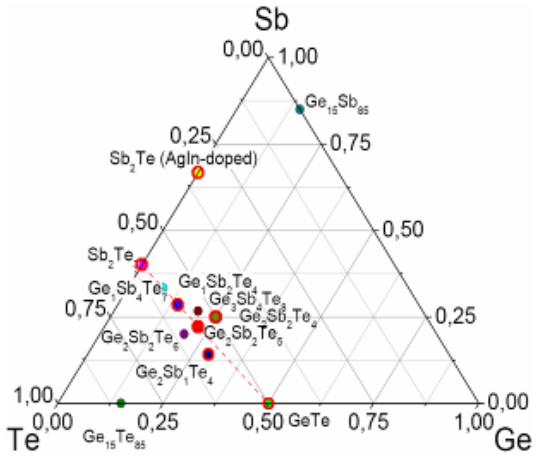
Basic idea:

• Optical memory disks use laser light to write small spots by converting the thin film back and forth from amorphous (disordered atomic structure) to crystalline (regular, highly repetitive, and ordered atomic structure). The digital data of 1s and 0s are stored as amorphous (high resistance and non-reflective) or crystalline (low resistance and reflective) structures.

• **PCM devices store data in a similar manner but use electrical energy controlled by small transistors to electronically convert the material to crystalline or to amorphous** (thus a 1 or a 0). This electronic solid-state memory stores data in a much smaller area and with higher speeds for both read and write than its optical counterpart.

Phase change materials

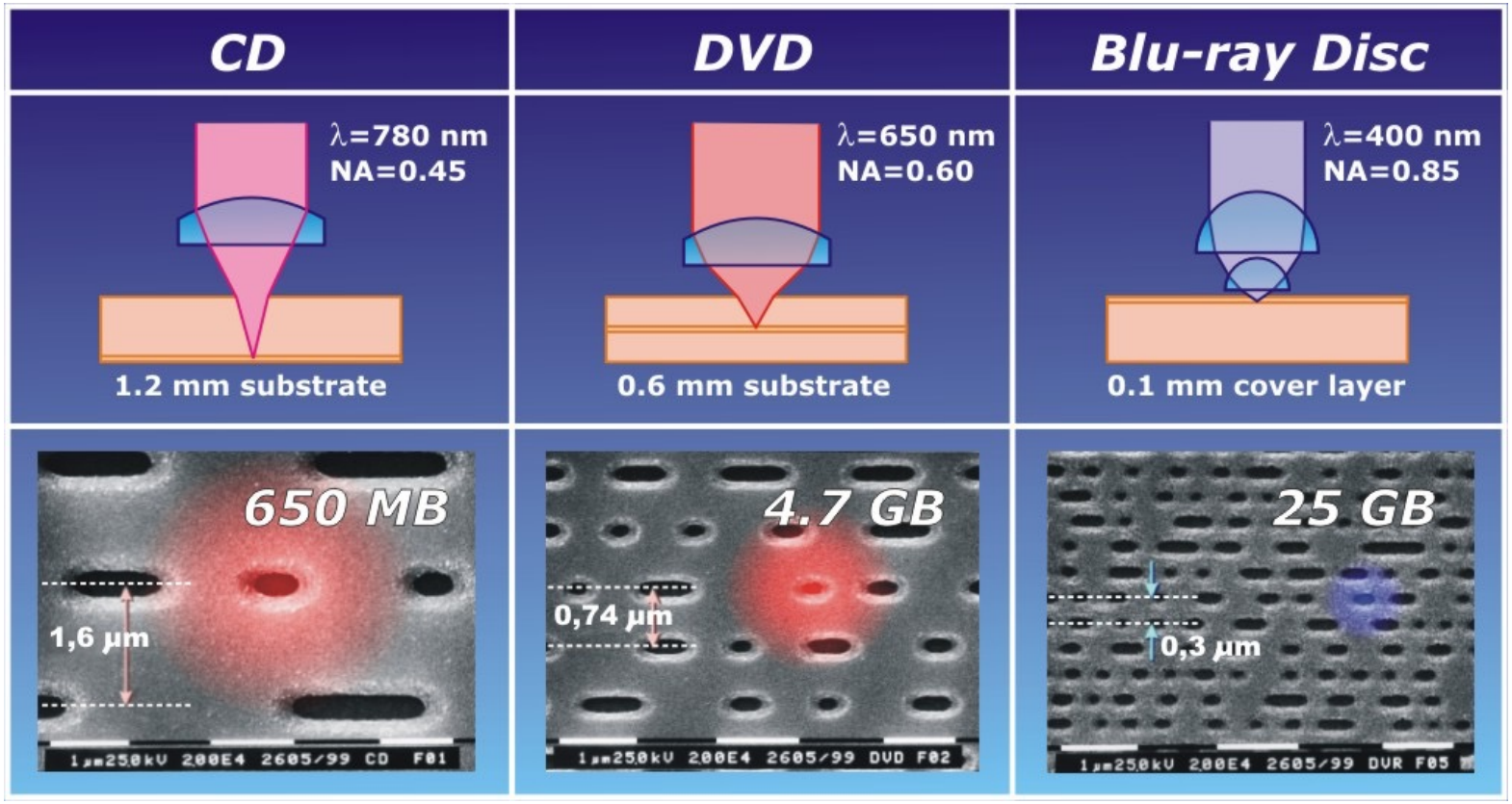




- Chalcogenide materials are alloys with an element of the VI group of the periodic table, usually combined with IV and V group elements (As_2S_3, As_2Te_3, $SnSb_2Te_4$, GeTe, Sb_2Te_3, $Ge_2Sb_2Te_5$…)

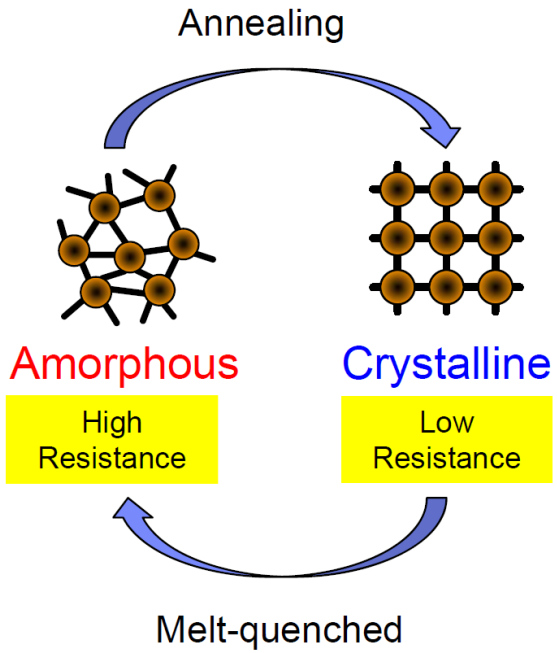
- Certain alloys containing one or more group VI elements (Chalcogenides) exhibit reversible transition between the disordered and ordered atomic structure

Optical storage: CD, DVD and Blu-ray disc

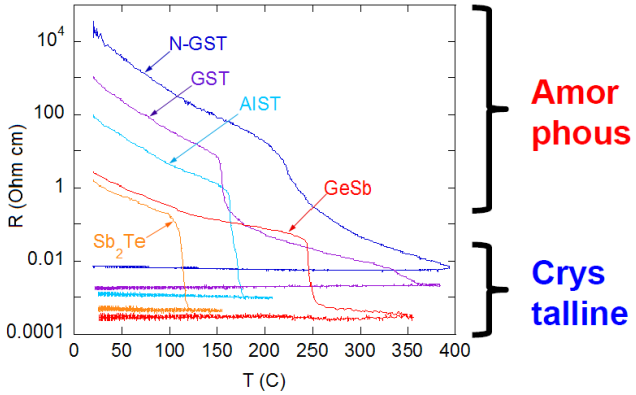


Phase Change Memory (PCM)

- Principle of Phase Change Memory: p**rogramming and reading the value of a material resistance**



[Various phase-change materials]
$Ge_2Sb_2Te_5$ (GST), AIST (AgInSbTe), GeSb, Sb_2Te and etc..

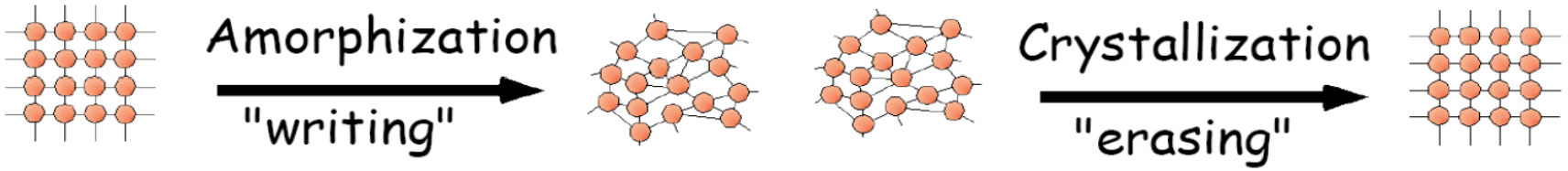


S. Raoux et al., *JAP*, v. 102, p. 094305, 2007.

- **Resistance change memory : ~1000X difference in resistivity**

Phase Change Materials

- **Same class of materials as the recording media of CD-RW and DVD-RW**
- **For DVD, a laser is used to write/erase by heating the GST**
  - High energy -> amorphous, low energy -> crystalline
  - Volume changes upon crystallization/amorphization changes the light scattered from the lower energy reading laser
- **For electrical phase change memory, the resistivity through the material is sensed by an external circuit**



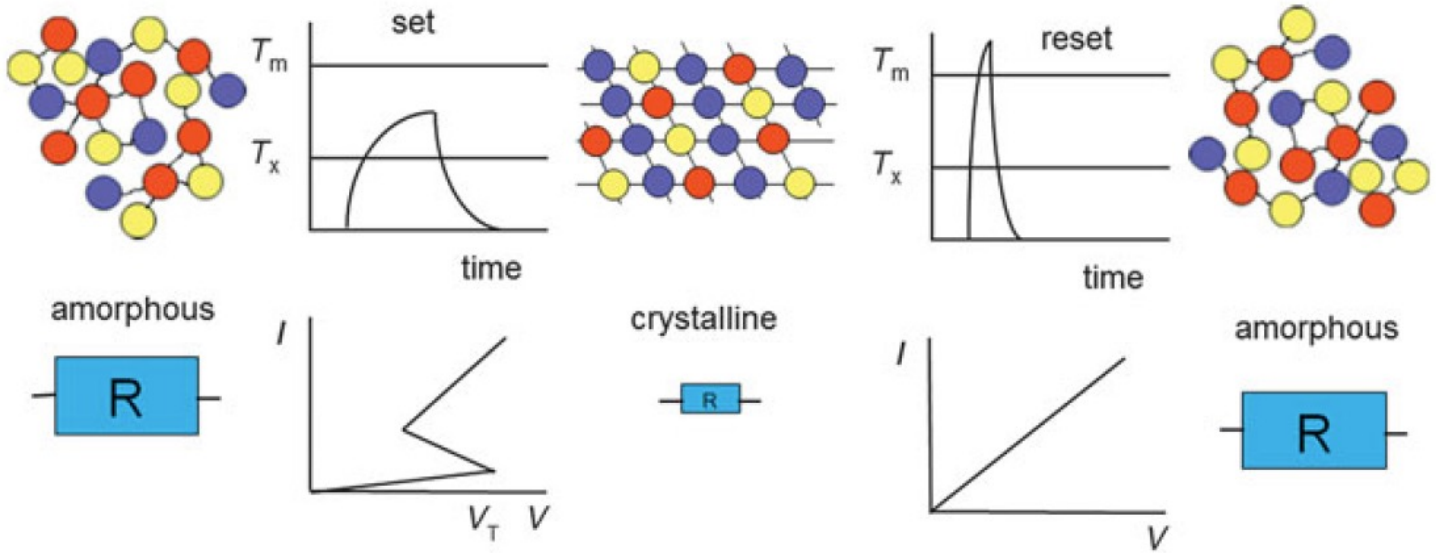
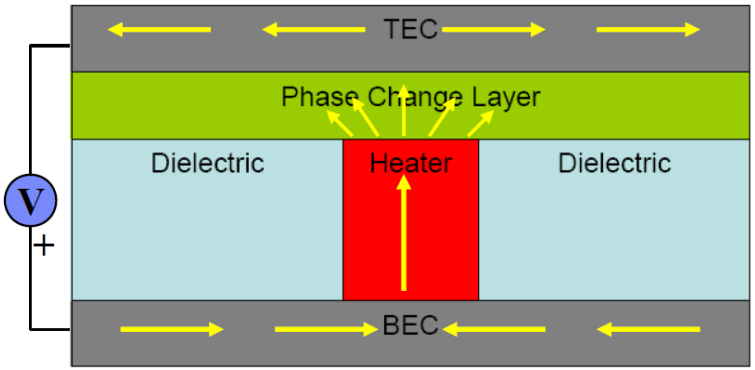
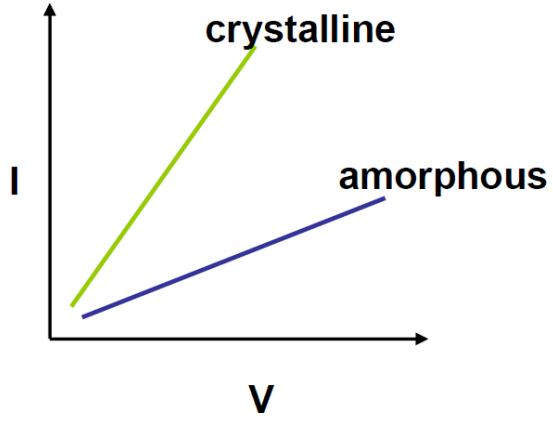


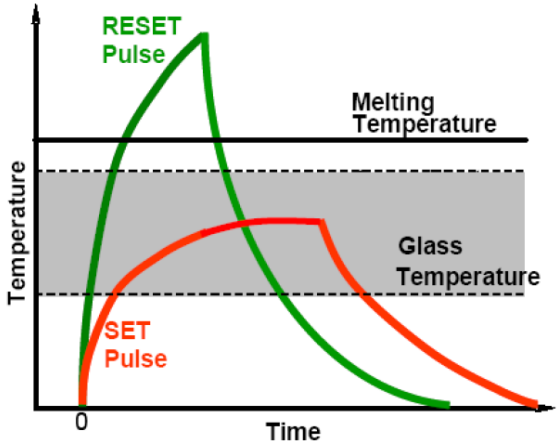
Figure 3. Principle of phase change memory. Starting from the amorphous phase with large resistance R, a current pulse is applied. At the threshold voltage V_T, the resistance drops suddenly, and a large current (I) flows that heats the material above the crystallization temperature T_x for a sufficiently long time to crystallize (set operation). In the crystalline state, the resistance is low. A larger, short current pulse is applied to heat the material above the melting temperature T_m. The material is melt-quenched and returns to the amorphous, high resistance state (reset operation). In the schematic, different colors represent different atoms (such as Ge, Sb, and Te in the commonly used GeSbTe compounds) in the phase change materials.

Principle

Operation Principle: Device operates by switching between *low resistance* SET state and *high resistance* RESET state.



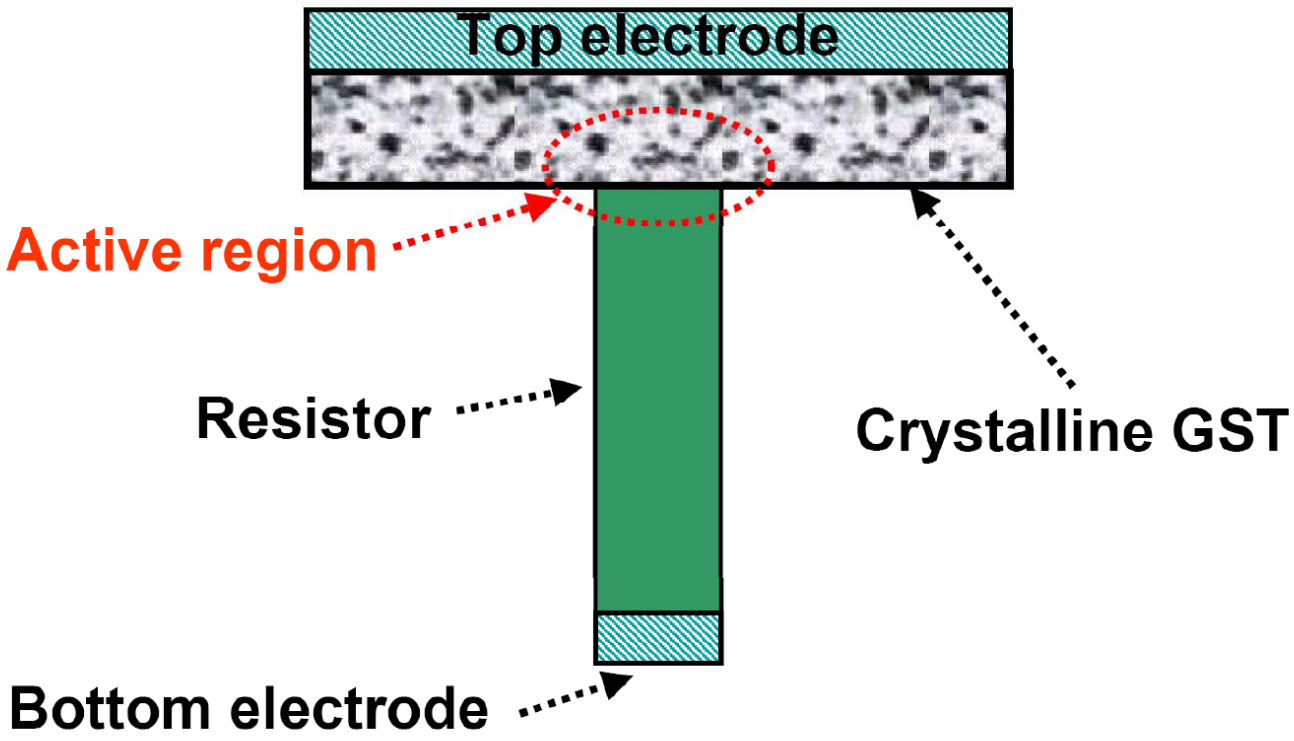




Electrical current pulses lead to intense localized heating (~10^{11}K/s) in the phase change layer.

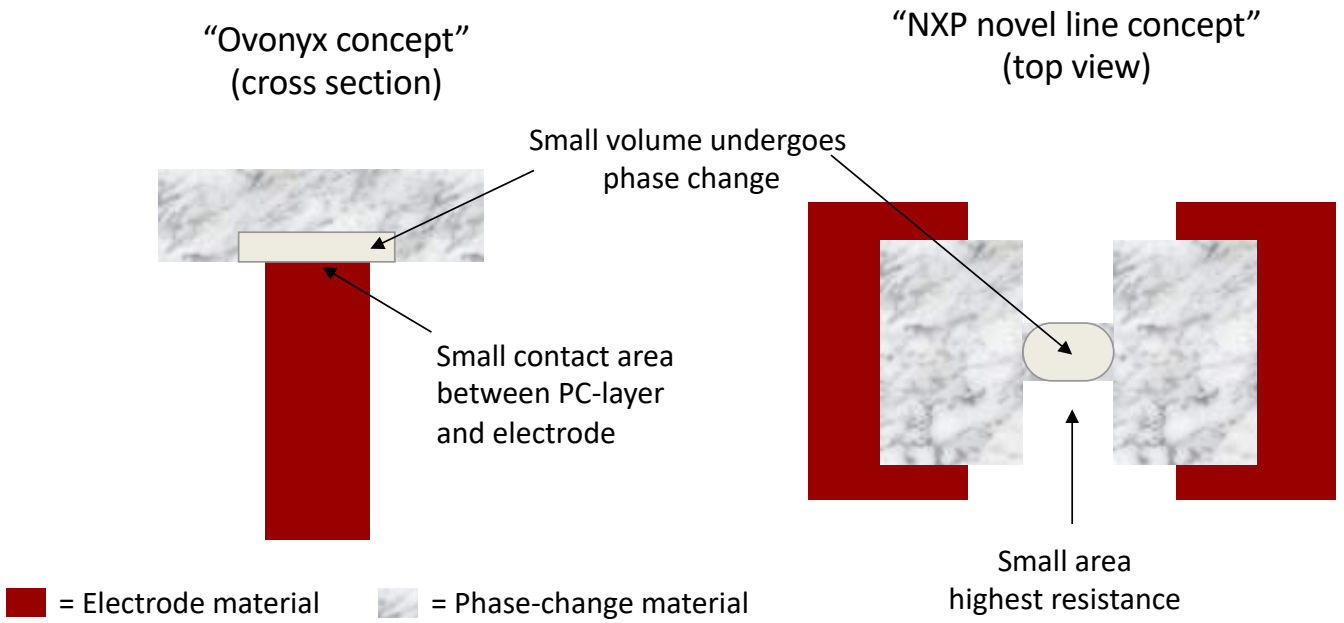
Controlled pulses cause transition between the high resistivity amorphous phase and low resistivity crystalline phase.

Typical PCM device



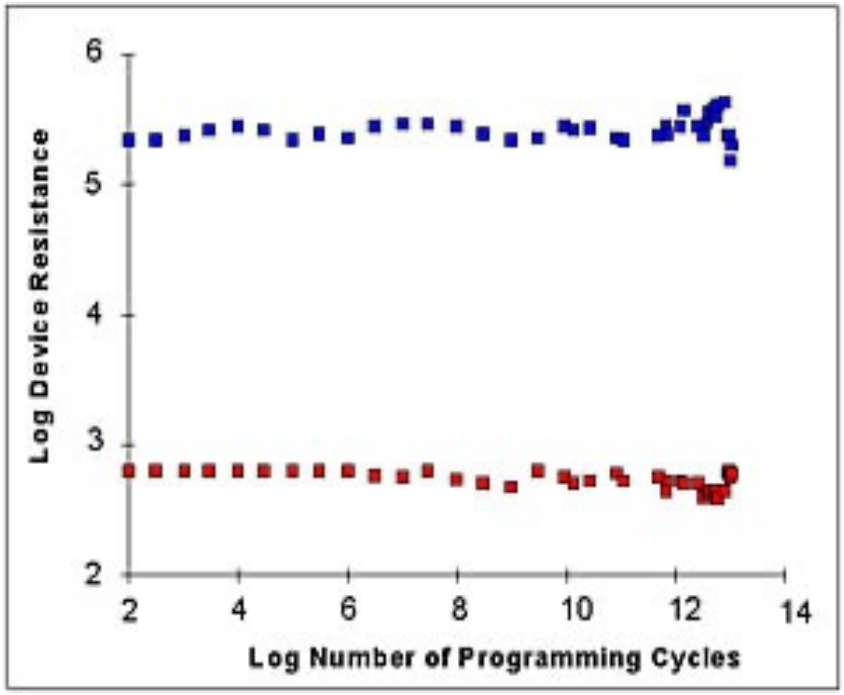
Cell concepts

- Megabit demonstrators by Intel, STM, Samsung → Ovonyx concept
- NXP Approach: Novel cell concept & Material

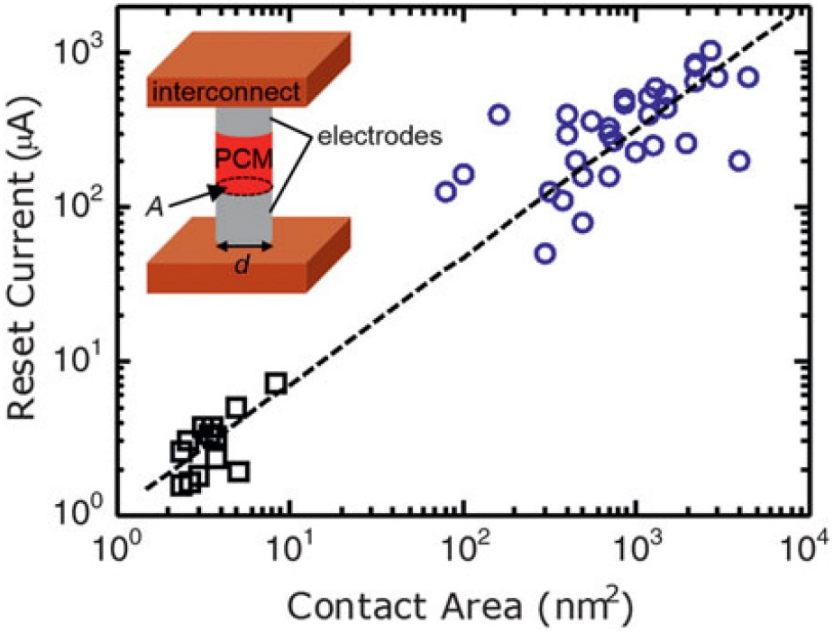


PCM endurance

• Fully random: any given bit can be uniquely addressed and then written or read by the customer. Further, Flash memory "wears out" (fails) after 100’000 write cycles, while the PCM memory state can be written more than 10 trillion times (real memory may fail faster), making this memory useful for program storage (Flash) as well as general purpose interactive (DRAM) data storage memory.



RESET current reduction needed!



- Typical high-performance transistor delivers drive current of 1mA/μm
- At 32nm node, for W/L=4, I = 128 μA

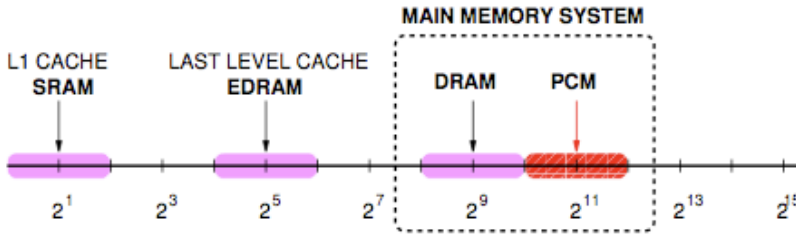
- It is capable of switching PCM with area of 100-150 nm^2

PCM advantages

- **Scales better than DRAM, Flash**
  - Requires current pulses, which scale linearly with feature size
  - Expected to scale to 9nm and beyond
  - Prototyped at <20nm
  - **Can be denser than DRAM**
  - Can store multiple bits per cell due to large resistance range

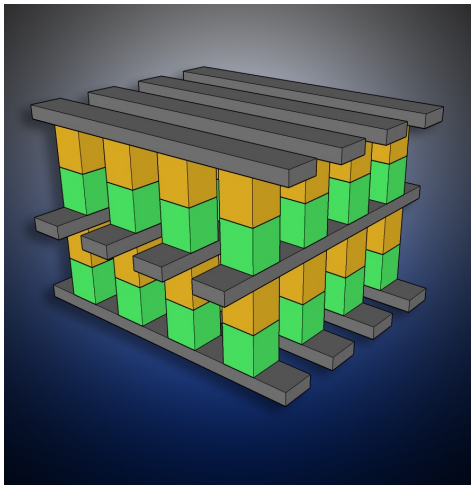
- **Non-volatile**
  - Retain data for >10 years at 85C
  - No refresh needed, low idle power

latency comparable but slower than DRAM:



Typical Access Latency (in terms of processor cycles

PCM products



3D XPoint technology developed jointly by Intel and Micron Technology.

- announced in July 2015
- available on the open market under the brand name **Optane** (Intel) from April 2017 to July 2022
- Discontinued in 2022

Uses germanium-antimony-tellurium (GST) as the data storage material

SSD commercialized in 2016-2022

Currently PCM - niche products (e.g. aviation, space - support ionizing radiation)
PCM ha s the potential to become one of principal memory solutions

PCM: specific issues and complications

- High programming current density (>10^7 A/cm^2, compared to 10^5 - 10^6 A/cm^2 for a typical transistors/diodes)

-The contact between the hot phase-change region and the adjacent dielectric (leakage, adhesion problems due to different thermal expansion)

-Long-term resistance and threshold voltage drift

PCM from stand-alone memory to new computation paradigms (IMC-chips)

Phase-Change Memory for In-Memory Computing

Published as part of Chemical Reviews special issue "Neuromorphic Materials".

Ghazi Sarwat Syed,* Manuel Le Gallo, and Abu Sebastian

Cite This: *Chem. Rev.* 2025, 125, 5163–5194

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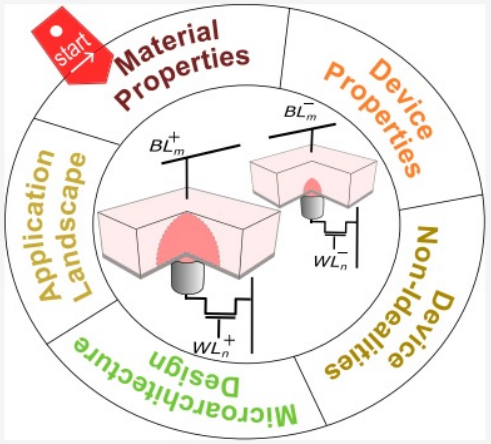
ABSTRACT: In-memory computing (IMC) is an emerging computational approach that addresses the processor-memory divide in modern computing systems. The core concept is to leverage the physics of memory devices and their array-level organization to perform computations directly within the memory array. Phase-change memory (PCM) is a leading memory technology being explored for IMC. In this perspective, we review the current state of phase-change materials, PCM device physics, and the design and fabrication of PCM-based IMC chips. We also provide an overview of the application landscape and offer insights into future developments.



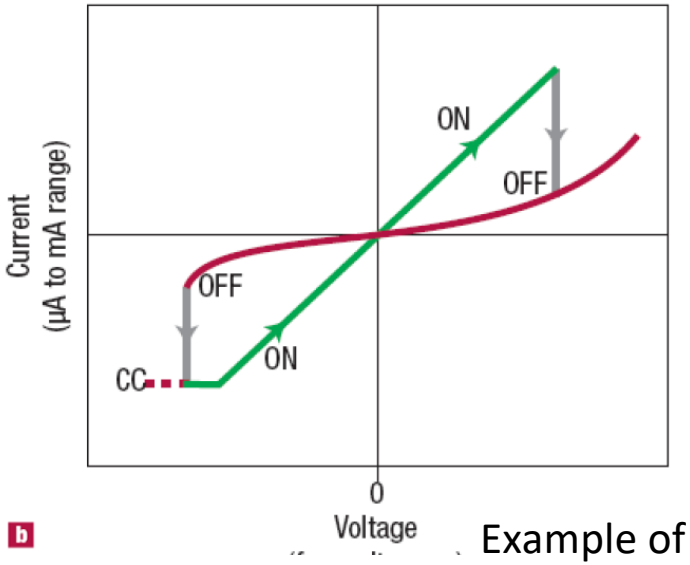
Summary: Pros and Cons

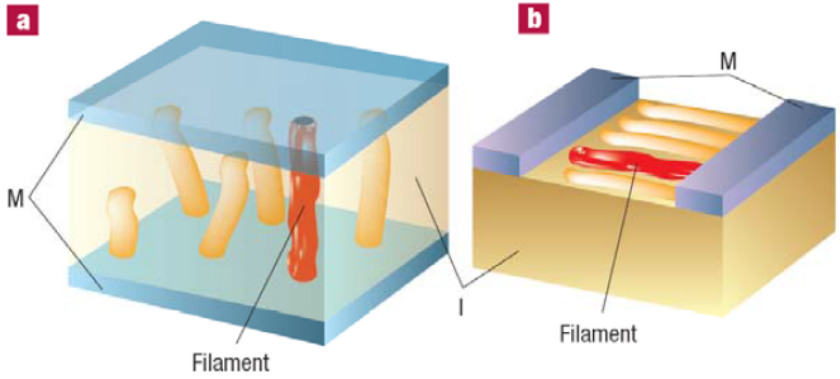
- **Pros over DRAM**
  - Better technology scaling
  - Non volatility
  - Low idle power (no refresh)
- **Cons**
  - Higher latencies: ~4-15x DRAM (especially write)
  - Higher active energy: ~2-50x DRAM (especially write)
  - Lower endurance (a real memory cell dies after ~10^8 writes)
  - Long-term resistance and threshold voltage drift – reliability issues

- **Challenges in enabling PCM as DRAM replacement/helper**:
  - Mitigate PCM shortcomings
  - Find the right way to place PCM in the system
  - Ensure secure and fault-tolerant PCM operation
  - Endurance

Resistive Switching M-I-M memories

Principle: formation of conductive filaments!



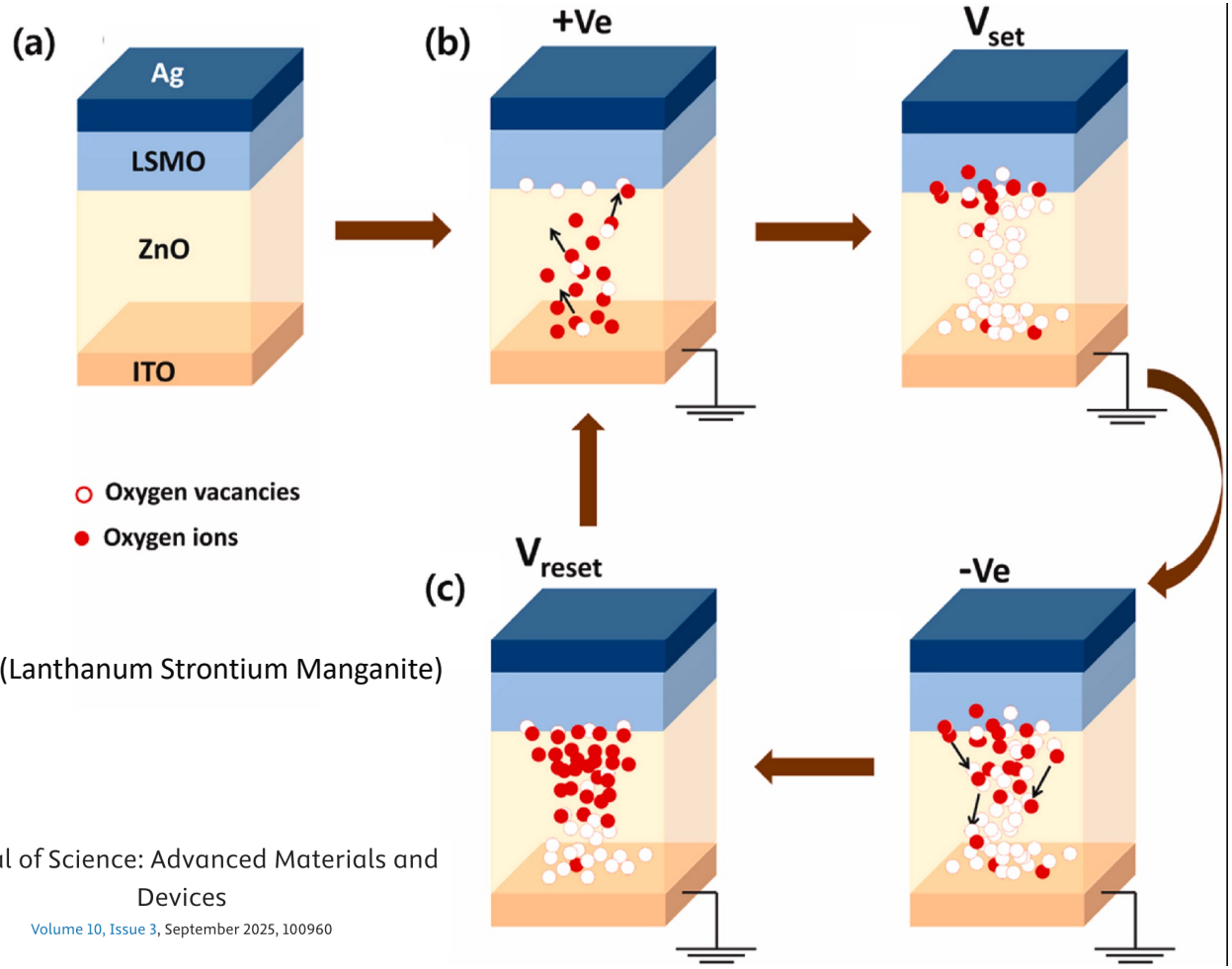


Example of possible defect chemistry reaction:
defficiency of oxygen in TiO_2 : ($TiO_{2-\delta}$) – loss of oxygen

$$O_O^{\times} \overset{TiO_2}{\leftrightarrow} \frac{1}{2} O_2(g) + V_O^{\bullet\bullet} + 2e'$$

This process is analogous to soft breakdown of oxides

Mechanisms of resistive switching



LSMO (Lanthanum Strontium Manganite)

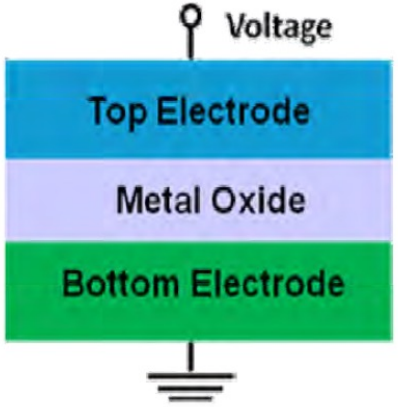
Journal of Science: Advanced Materials and Devices
Volume 10, Issue 3, September 2025, 100960

- The dielectric layer initially contains a substantial number of randomly dispersed oxygen vacancies (a)
- When a positive bias is applied to the TE (b), these vacancies migrate toward the BE, facilitating conductive filament growth and changing the device from HRS to LRS
- In contrast, a negative bias disrupts the conductive path (c), returning the device to HRS and representing the RESET step

Mechanism based on formation and rupture of filaments, and its charge carriers emerge from oxygen vacancy migration and oxidation within the dielectric layer when an external bias is applied

Metal-Oxide M-I-M memory (RRAM)

- **Motivation:**
  - Low programming voltage (< 3V)
  - Material set compatible with conventional semiconductor processing (e.g Ni, Hf, Al…)
  - Low temperature processing (BEOL-compatible)



New functionalities:

-RRAM is can be suitable for neuromorphic circuits

- reliability issues still need to be addressed

fatigue

stochastic formation of filament (scaling limitation)

RRAM: different concepts, materials, devices

Journal of Science: Advanced Materials and Devices

Volume 10, Issue 3, September 2025, 100960

Review Article

ices

Recent advances in resistive switching memory devices based on diverse material platforms for next generation electronics

Wonseop Shin [a], Sungho Jang [a], Hyojung Kim [b]

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Metal-Oxide M-I-M memory (RRAM)

Qualcomm introduces new IOT chipsets with embedded RRAM memory

Qualcomm Technologies has announced two new IOT chipsets, the Qualcomm QCC730M and Qualcomm QCC74xM modules. The company says that these modules are perfectly suited for IoT applications in the smart home, smart appliances and more.

The QCC730M chip is is a dual-band, micro-power Wi-Fi 4 module. Offering a dedicated 60Mhz MCU units, 640kB of SRAM and 1.5Mb RRAM memory. The QCC730M also integrates hardware crypto accelerator, and secure boot, debug, and storage.

Source: Qualcomm

2024 Niche Products are available

- **A number of companies are active in the field:**
- **Panasonic**
- **Fujitsu**
- **SanDisk** (Western Digital) develop RRAM memory including stand-alone applications like high-performance SSDs.

Embedded RRAM (eRRAM)
- Adopted by major foundries as **low-cost embedded NVM**
- Volume production at **40 / 28 / 22 nm**
- **12 nm qualified, 6 nm under development**

TSMC:
https://investor.tsmc.com/static/annualReports/2024/english/pdf/2024_tsmc_ar_e_ch5.pdf?utm_source=chatgpt.com

MRAM (Magnetic RAM)

or STT-RAM (Spin-Transfer Torque RAM)

or STT-MRAM

Giant Magnetoresitive Effect (GMR)

- Discovered in 1988 by Albert Fert's group in France (Fert & Grunberg 2007 Nobel prize)
- Observed in artificial thin-film materials composed of alternate **ferromagnetic and non-magnetic layers**:
  - **RESISTANCE of the material is the LOWEST when magnetic moments of the ferromagnetic materials are ALIGNED**
  - **RESISTANCE of the material is the HIGHEST when the magnetic moments of the ferromagnetic materials are ANTI-aligned**

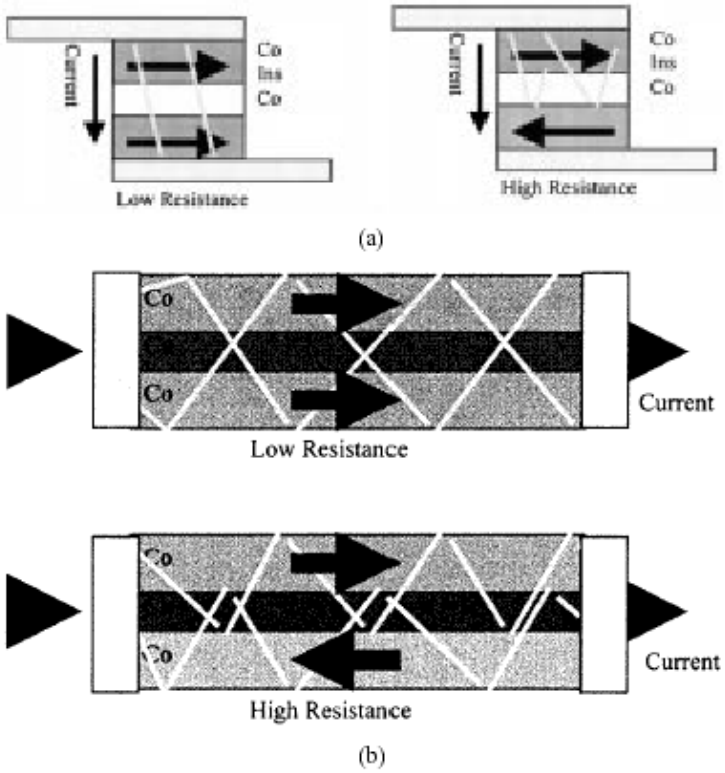


Fig. 2. Comparison of spintronic devices where current is (a) Perpendicular to the Plane (CPP) and (b) Current is In-Plane (CIP).

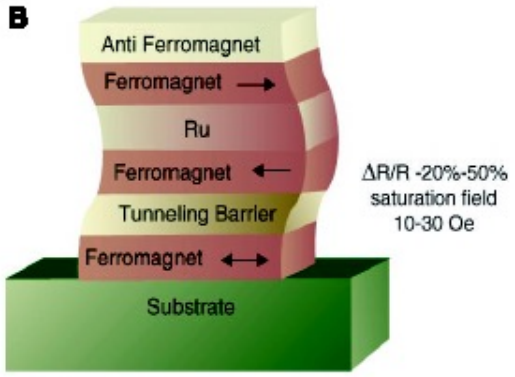
Magnetic Tunnel Junction (MTJ) for STT-RAM

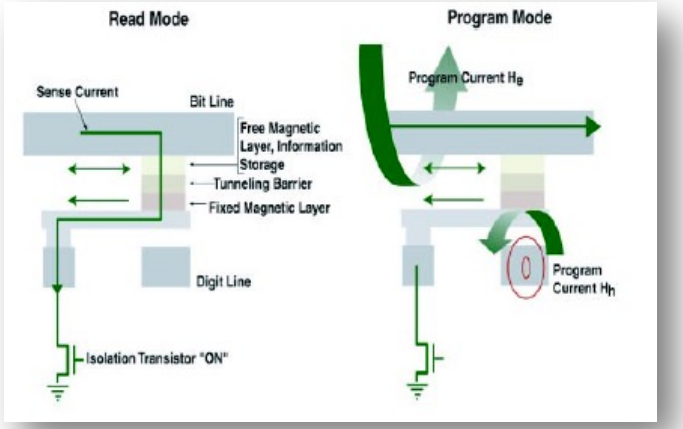
- **Magnetic Tunneling Junction**:

  - A device in which a pinned layer and a magnetic layer are separated by a very thin insulating layer (Al2O3).

  - The **tunneling resistance is modulated by the magnetic field**, exhibiting 20-40% in magneto-resistance change.

- Use such a cell to build a **Spin-Transfer Torque RAM (STT-RAM) memory to replace DRAM!**

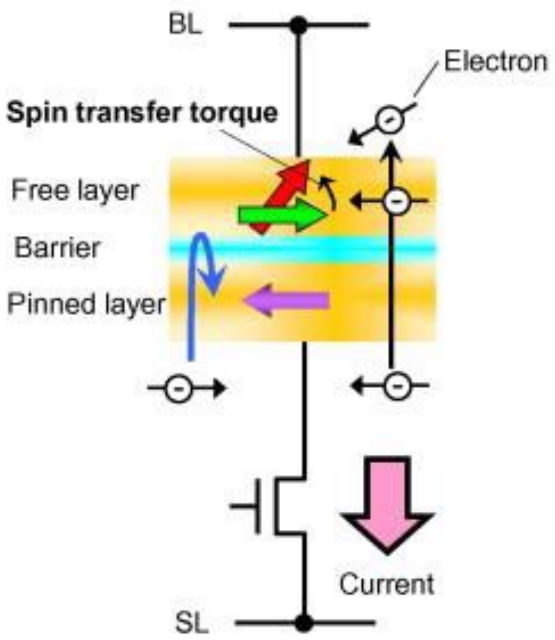




STT-RAM: writing principles

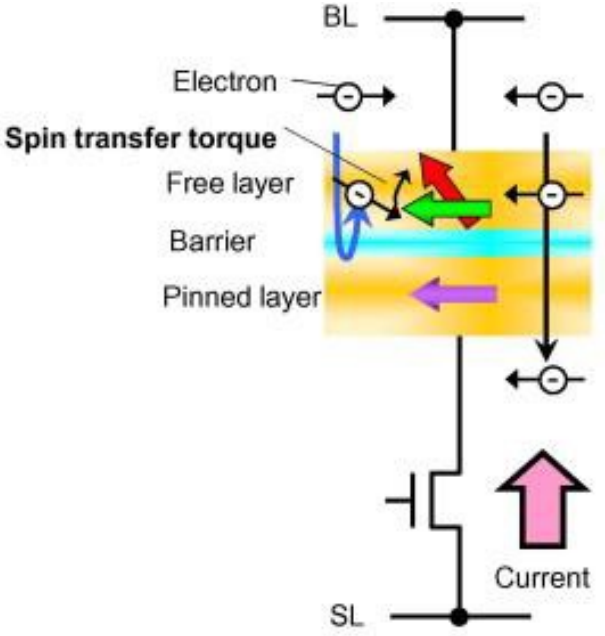
Important: pinned layer (fixed magnetization) and free layer (switchable)

Antiparallel to parallel
The spin-polarized current exerts STT on the free layer



(a) Anti-Parallel (AP) to Parallel (P) switching

parallel to anti-parallel switching
Electrons with the same spin as the pinned layer pass though, but electrons with opposite spins are reflected



(b) Parallel (P) to Anti-Parallel (AP) switching

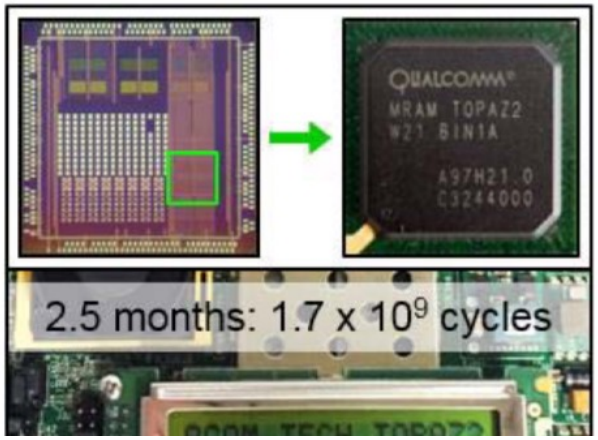
MRAM: high write endurance

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 9, SEPTEMBER 2017 3639

A Study on Practically Unlimited Endurance of STT-MRAM

Jimmy J. Kan, Chando Park, Chi Ching, Jaesoo Ahn, Yuan Xie, *Fellow, IEEE*, Mahendra Pakala, and Seung H. Kang

***Abstract*— Magnetic tunnel junctions integrated for spin-transfer torque magnetoresistive random-access memory are by far the only known solid-state memory element that can realize a combination of fast read/write speed and high endurance. This paper presents a comprehensive validation of high endurance of deeply scaled perpendicular magnetic tunnel junctions (pMTJs) in light of various potential spin-transfer torque magnetoresistive random-access memory (STT-MRAM) use cases. A statistical study is conducted on the time-dependent dielectric breakdown (TDDB) properties and the dependence of the pMTJ lifetime on voltage, polarity, pulsewidth, duty cycle, and temperature. The experimental results coupled with TDDB models project $>10^{15}$ write cycles. Furthermore, this work reports**



However the endurance of MRAM can be affected by write current (high current = high probability of junction breakdown) – such reports are to be considered with some criticism…

STT-RAM state of art

	FLASH	MRAM	PCM	RRAM
Programming power	~200pJ/bit	~20pJ/bit	~300pJ/bit	~100pJ/bit
Write speed	20µs	20ns	10-100ns	10-100ns
Endurance	10^5-10^6	10^6-10^{15}	10^7-10^8	10^5-10^7
Retention	>125°C	85-215°C	165°	>125°
Extra masks	Very high >10	Limited (3-5)	Limited (3-5)	low (2)
Bias Usage (HV)	High	low	medium	low
Process flow	Complex	medium	medium	simple
Scalability	bad	medium	high	high

Assessment of STMicroelectronics, 2021

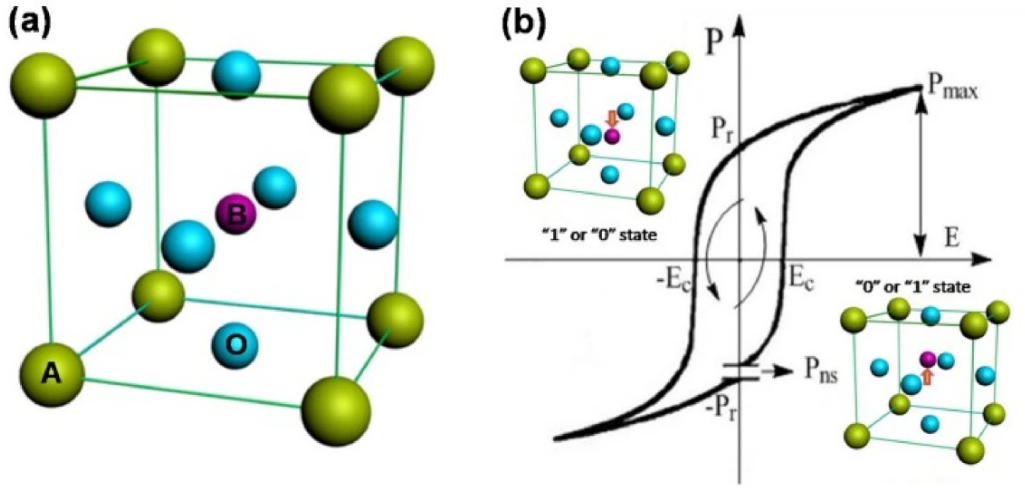
TSMC is currently offering 22nm eMRAM option as an eFlash alternative; the company is also looking to develop 14/12 nm eMRAM option to replace SRAM memory

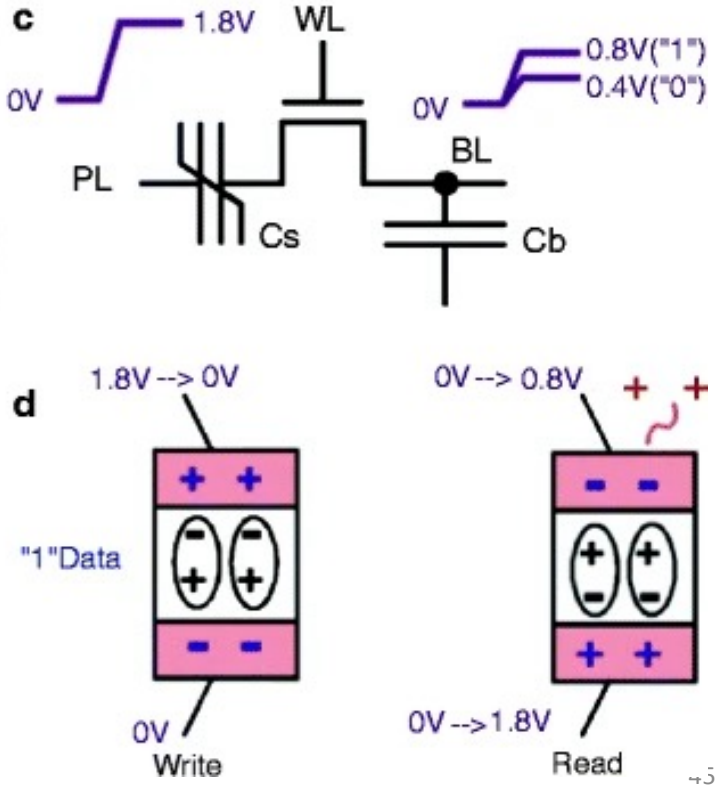
Industrial nodes: 22 nm, development toward 16/14/12 nm, high endurance, fast write/read, CMOS BEOL compatibility

Ferroelectric RAM (FRAM)

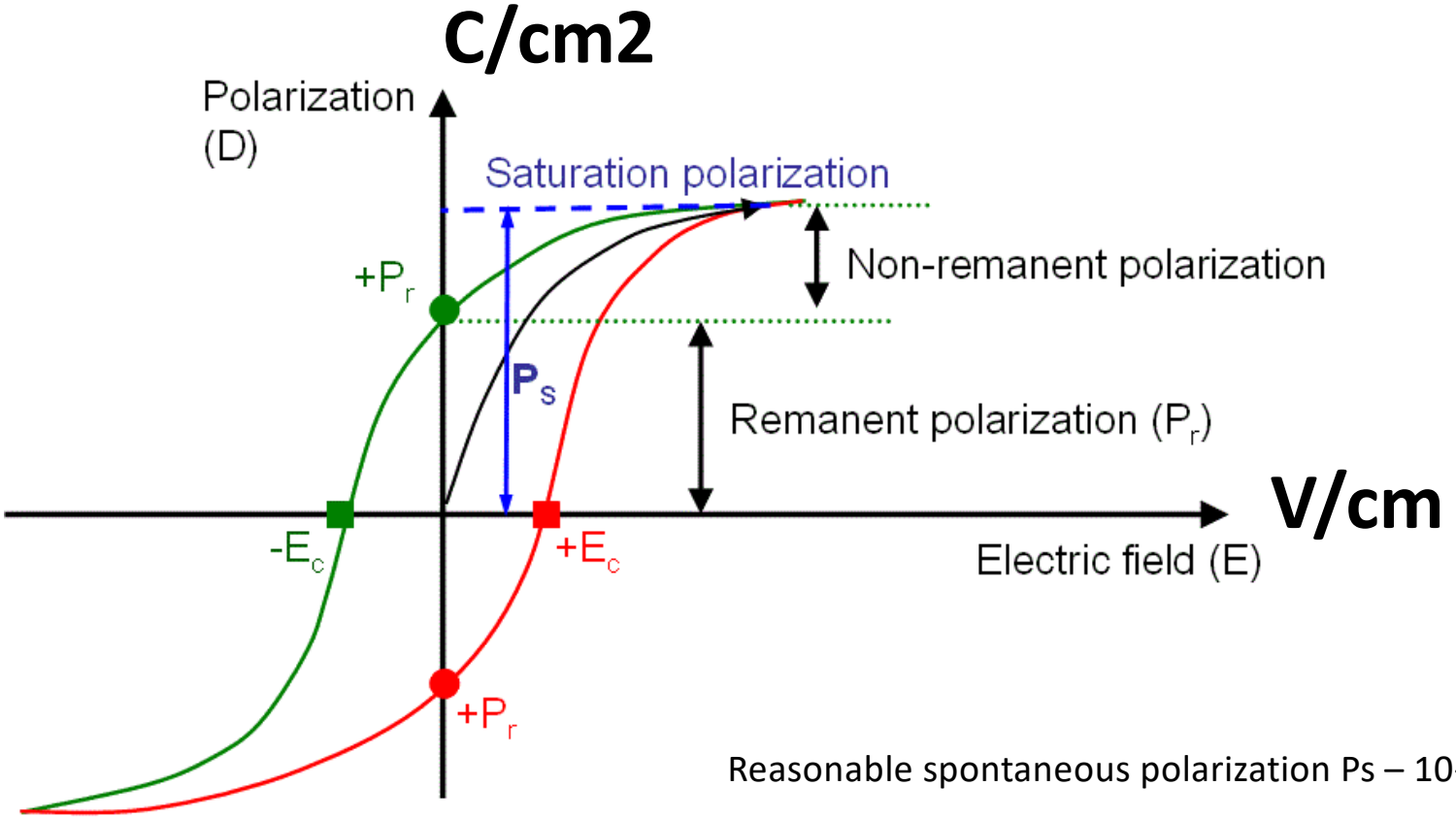
• A non-volatile memory concept based on ability of ferroelectric materials to electrically switch and maintain the spontaneous polarization

• Two types of FRAM:
- ferroelectric capacitors (instead of conventional dielectric capacitors like in DRAM)
- ferroelectric gates in FETs





The hysteretic characteristic of ferroelectrics is used to build ferroelectric memories

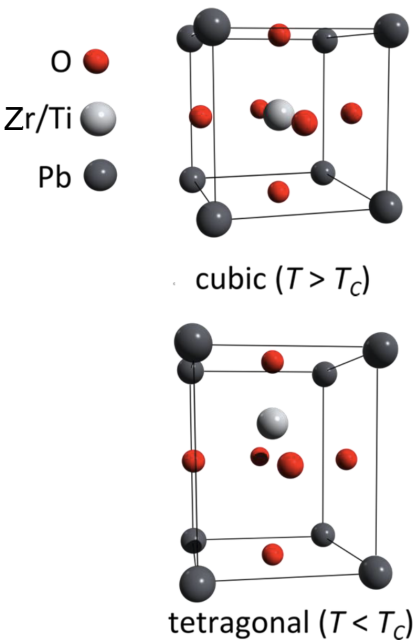


Reasonable spontaneous polarization Ps – 10-20 μC/cm^2

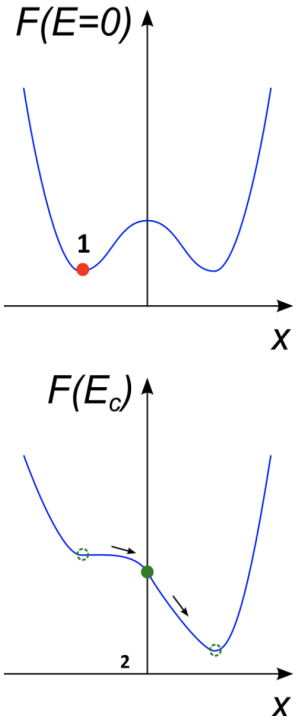
Ferroelectric materials

Ferroelectricity, property of certain dielectrics, that exhibit **spontaneous electric polarization** (separation of the centre of positive and negative electric charge, making one side of the crystal positive and the opposite side negative) that **can be reversed in direction by the application of an appropriate electric field**.

Ferroelectric crystal

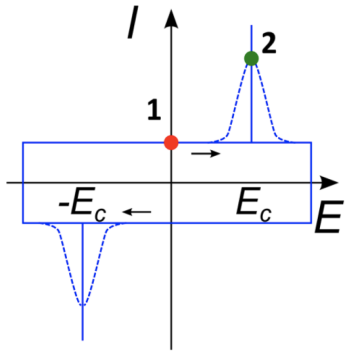


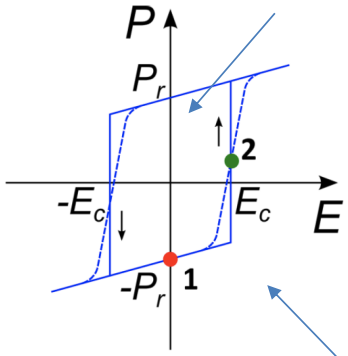
Double well potential of ferroelectric material



Hysteresis

$$P = \frac{1}{A}\int I\,(t)\,dt$$



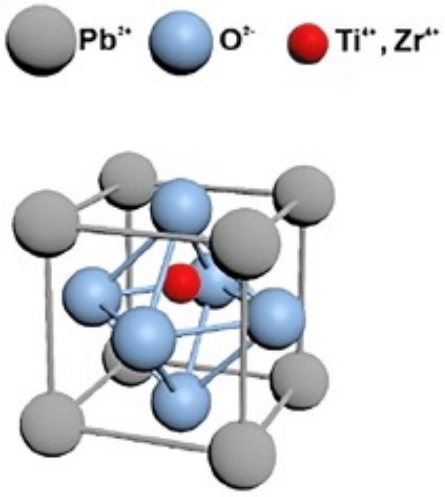
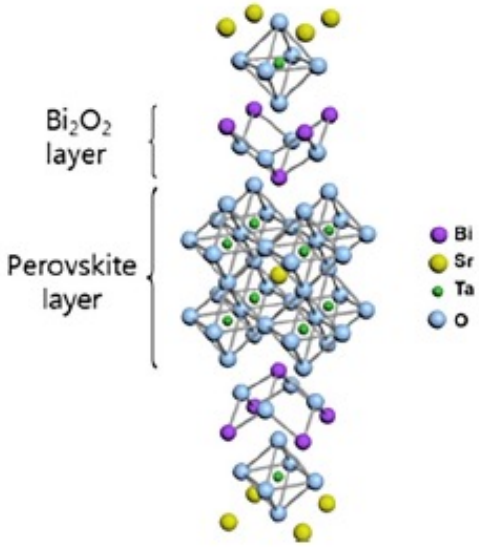
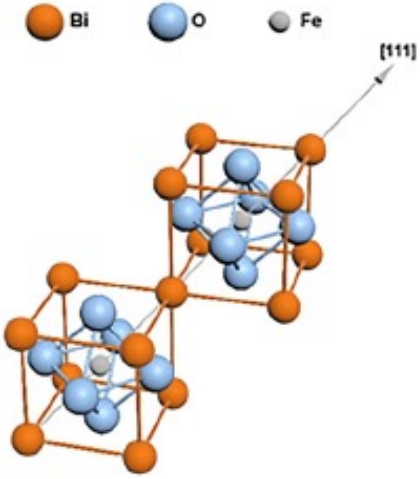


remanent Polarization, Pr

coercive field, Ec

Ferroelectrics have two stable polarization states that can be switched by an electrical field.

Perovskite type ferroelectrics for FRAMs

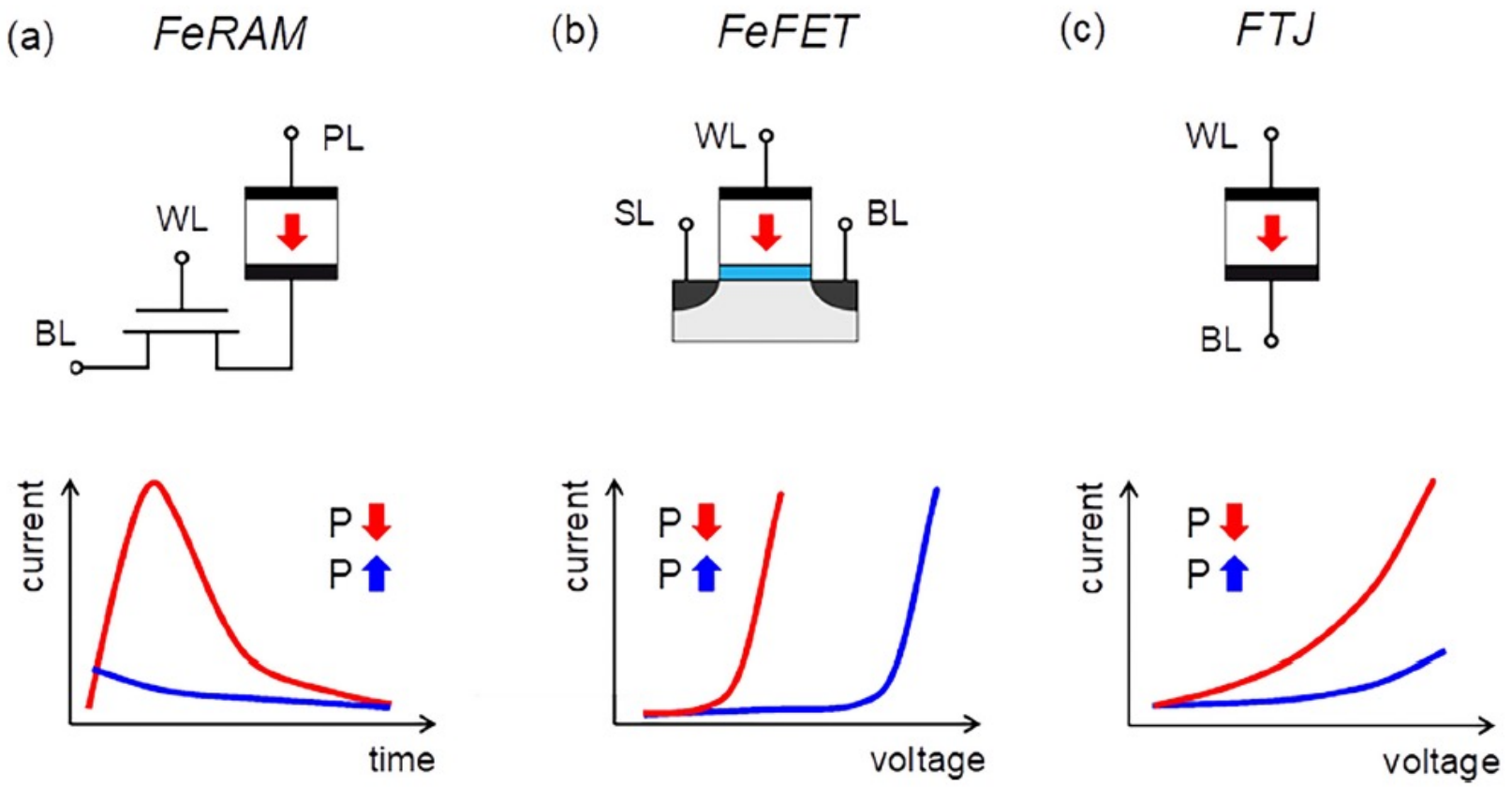
Ferroelectrics	$Pb(Zr,Ti)O_3$	$SrBi_2Ta_2O_9$	$BiFeO_3$
	Perovskite (Tetragonal)	Layered-perovskite (Tetragonal)	Perovskite (Rhombohedral)
Crystal structure			

FRAM memory concepts

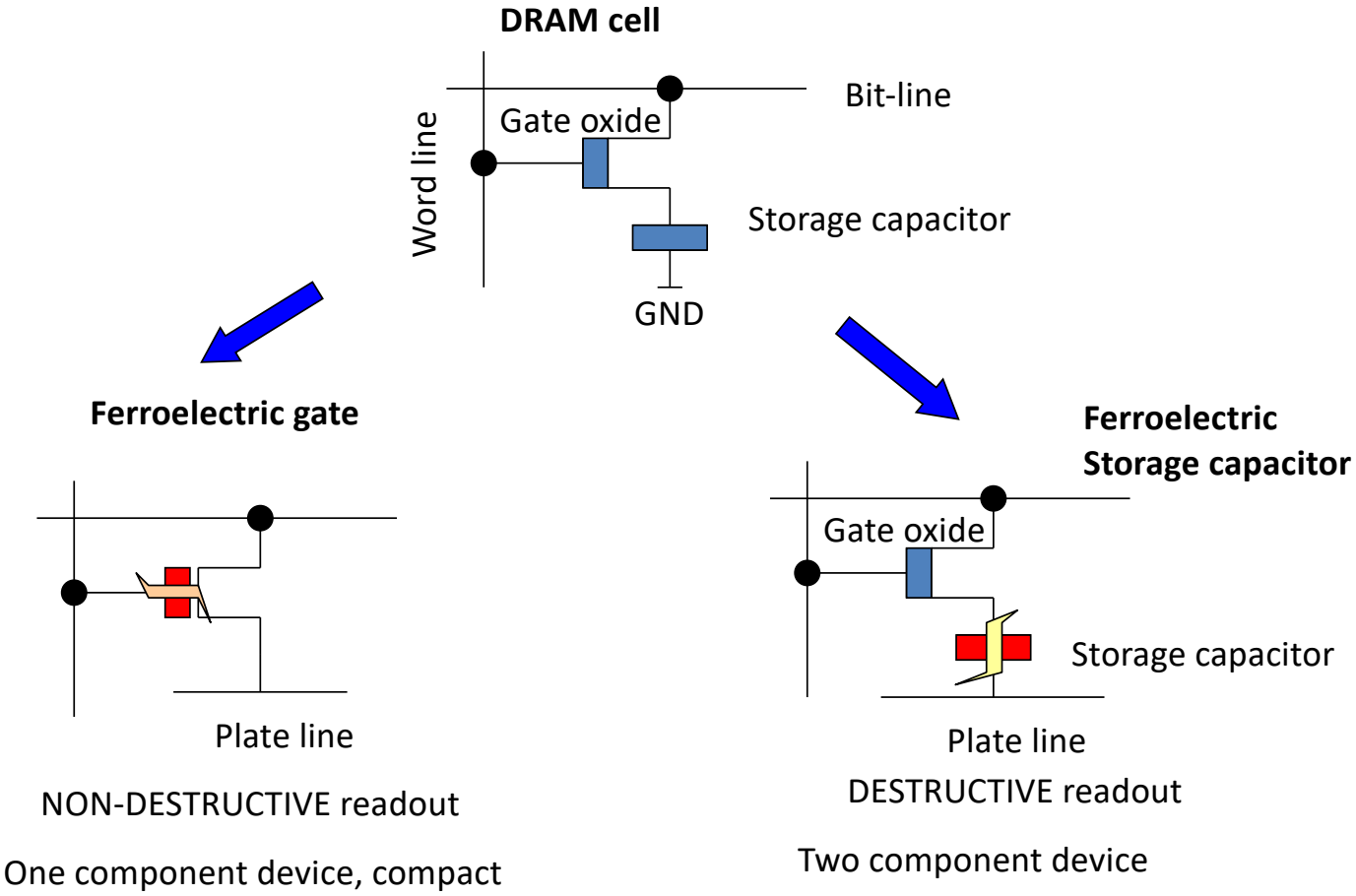
Capacitor

FET

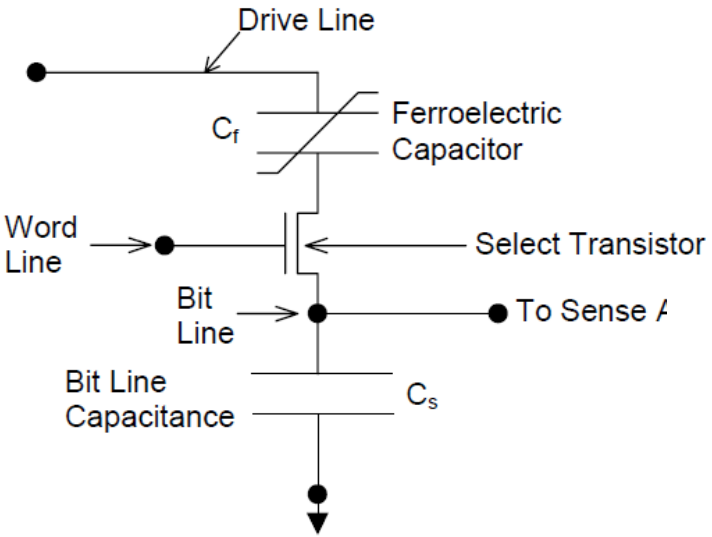
Tunnel Junction

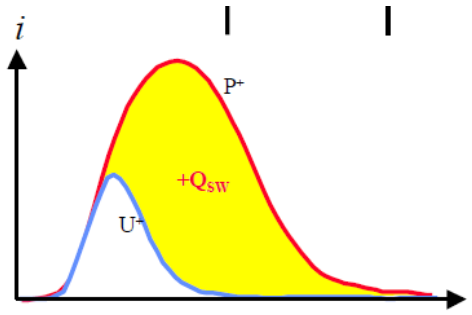


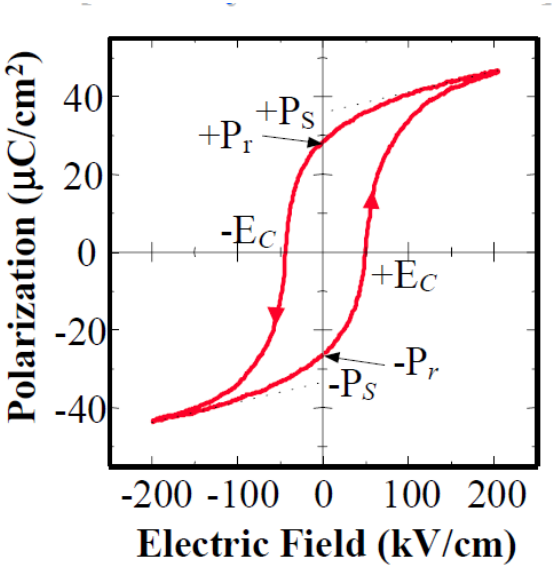
Types of Ferroelectric RAM (ferroelectric capacitors vs. FeFETs)



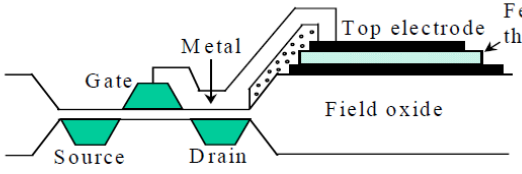
1T-1C cell principle



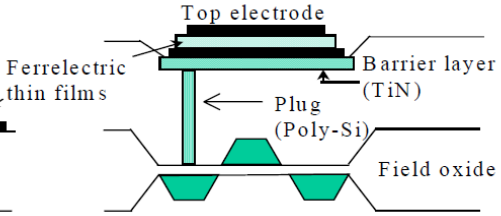




P_S : Spontaneous Polarization
P_r : Remanent Polarization
E_C : Coercive Field



Low density memory device
(64 Kbit)



High density memory device
(1 Mbit)

Particular feature of FRAM : good resistance against ionizing radiation (space applications)

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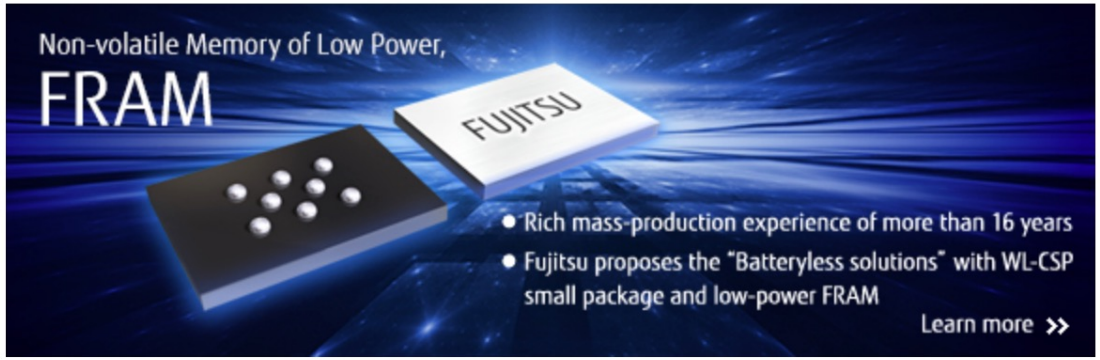
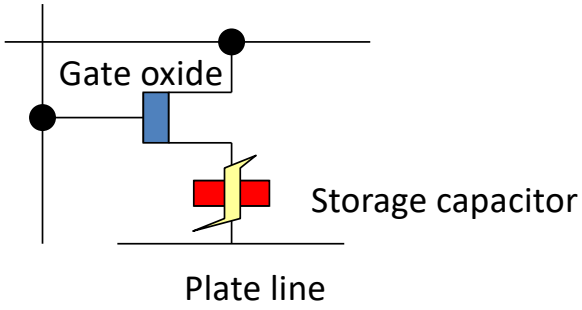


Topics Back numbers >>

- Mar. 3, 2016 Added a topic of "FRAM employed in a satellite."
- Feb. 29, 2016 Released a video introducing "3 Reasons Customers Choose FRAM."

1T1C FRAM
(destructive readout)



Advantages:

- Truly non-volatile
- No intervention on the silicon level
- Easier to process than MFS structures

Disadvantages:

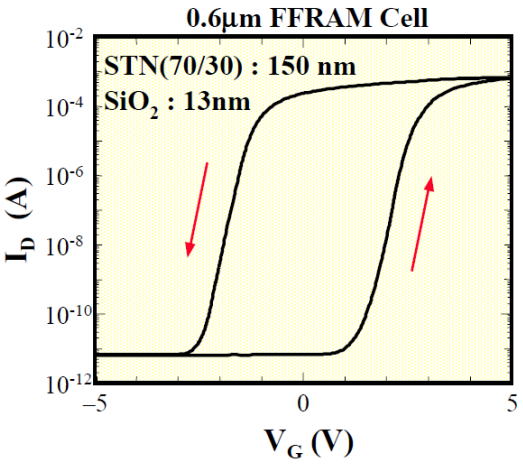
- Switching required for read-out
- A number of reliability issues

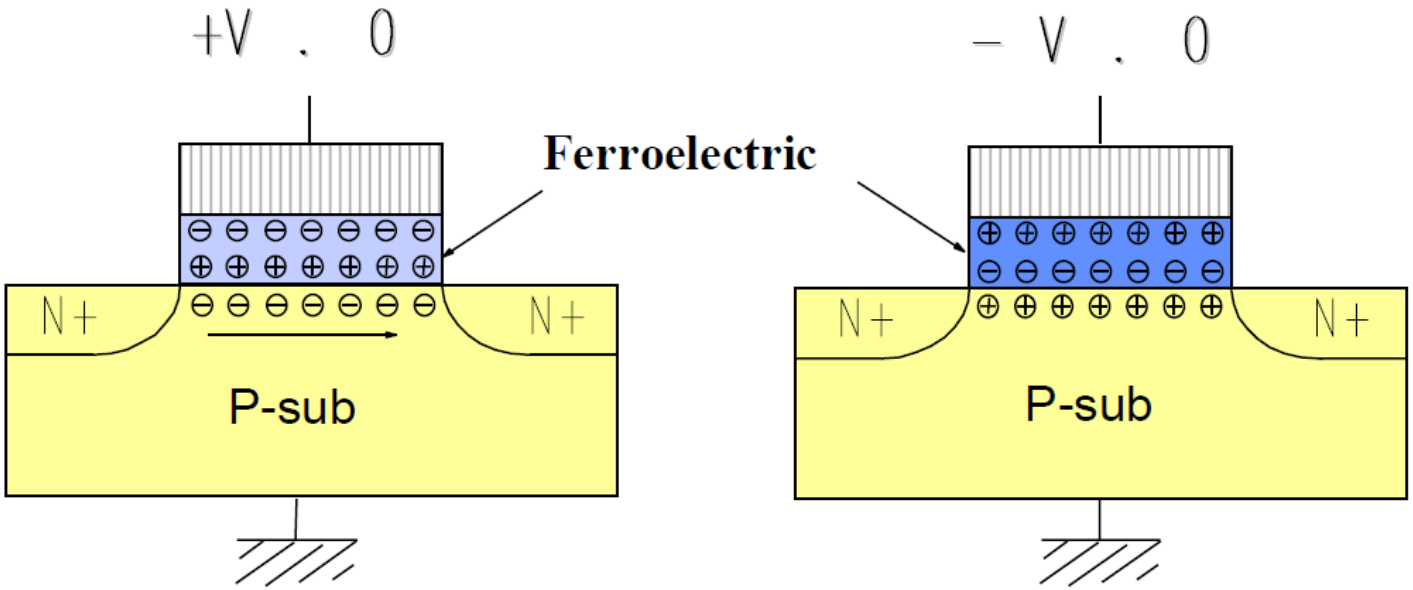
Reliability issues:

- Polarization Fatigue
- Retention Loss
- Imprint
- Integration

1T-FeRAM cell: principle

[Memory Window]



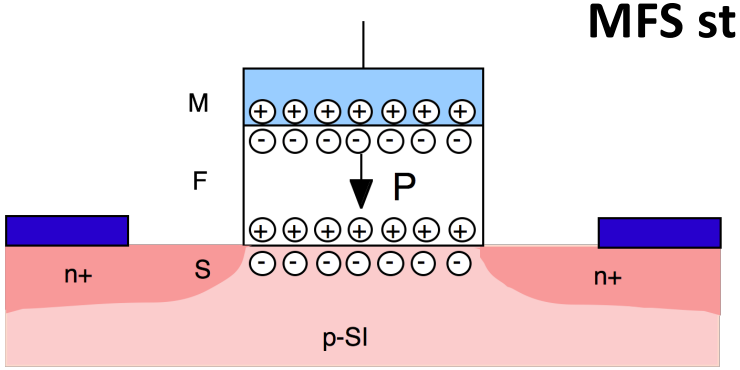


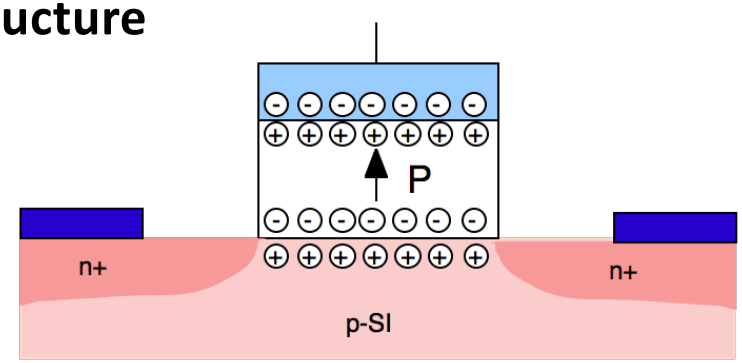
"on state"

"off state"

FRAM with non-destructive readout ferroelectric FET

MFS structure





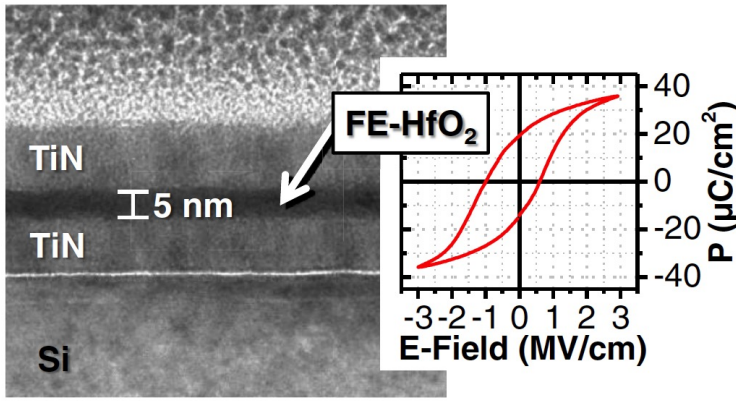
ON-state: An inversion state is formed in the channel, the polarization charges are compensated by electrons (minority carriers): Low resistance

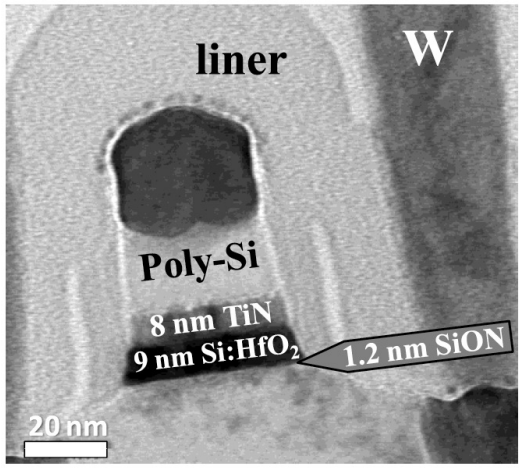
Off-state: The polarization charges are compensated by holes. One of the pn junctions is in reversed direction: High resistance.

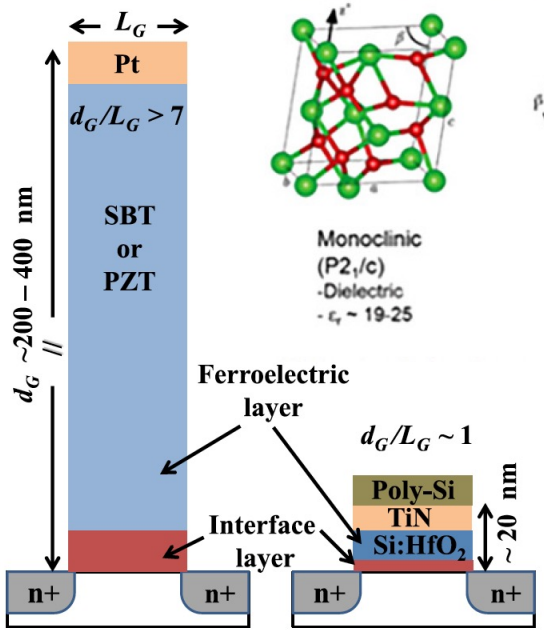
Problems:

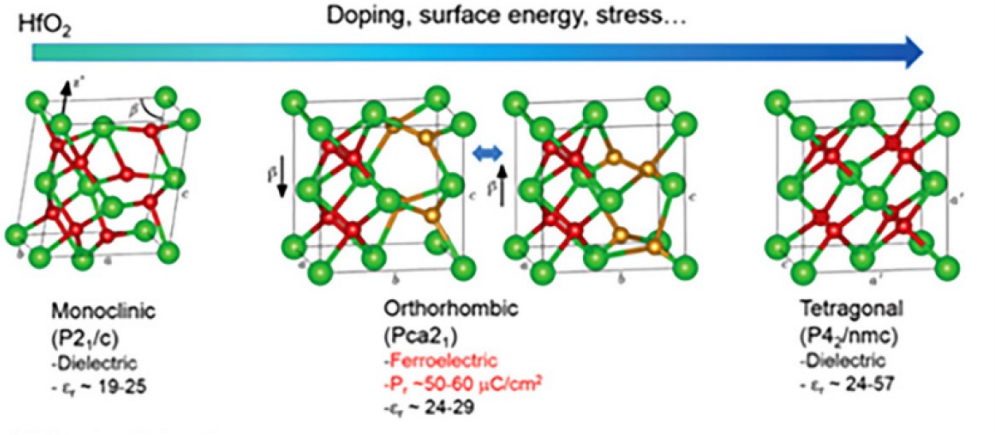
1) Processing: The ferroelectric-silicon interface is badly defined. Charge traps. Formation of SiO_2: low ε dielectric layer. A buffer layer e.g. HfO_2 is needed
2) Charge compensation by leakage: The field effect is diminishing with time. The device is not really non-volatile

Emerging CMOS-compatible ferroelectrics, doped HfO_2 : new opportunities for FRAMs







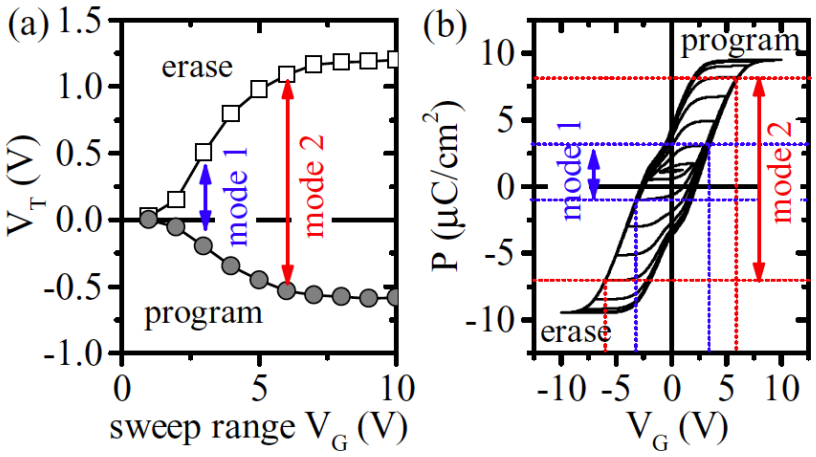


J. Muller et al., ECS Journal of Solid State Science and Technology, 4 (5) N30-N35 (2015)

Performance of HfO_2-based FRAM (28 nm)

Table III. Performance of FE-HfO_2 based 1T-1C and 1T concepts for different operating schemes.

Cell concept	Operating mode	Read endurance	Write endurance	Retention
1T-1C	FRAM	$\sim 10^9$	$\sim 10^9$	>10 y
	DRAM	unlimited	unlimited	<1 s
1T	Mode 1 (low V_G)	unlimited	10^{14}	$<10^3$ s
	Mode 2 (high V_G)	unlimited	10^4–10^5	>10 y



J. Muller et al., ECS Journal of Solid State Science and Technology, 4 (5) N30-N35 (2015)

HfO_2-based FRAM – recent developments

NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer,

Report from Micron Technology, IEDM 2023

Operation: -40°C – 90°C; 10 years retention

NVDRAM 32Gb

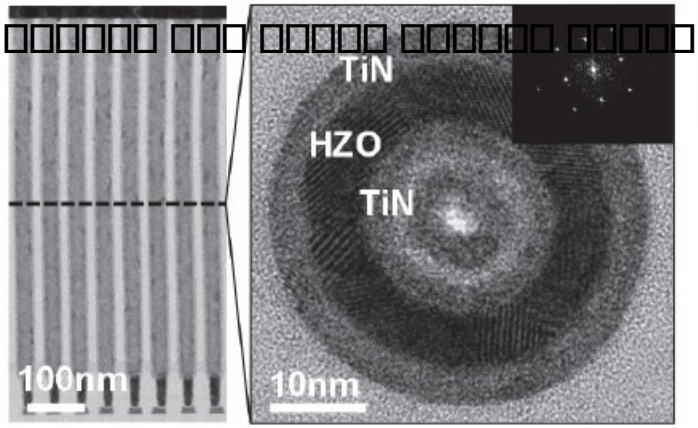


Figure 8. SEM cross-section of memory cells (left) and plan-view TEM showing TiN electrodes and crystalline ferroelectric (right).

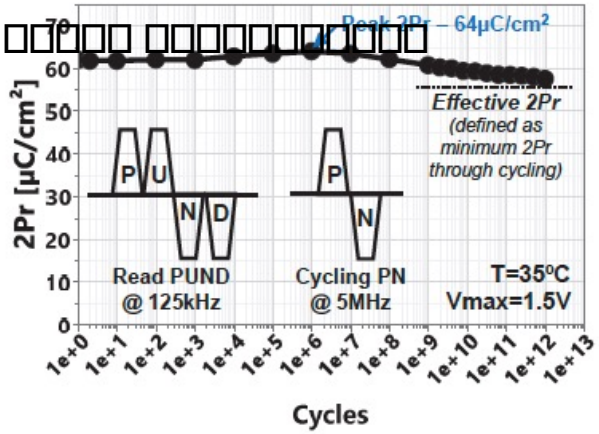


Figure 9. Polarization versus cycles up to 10^{12} (1.5V, 35°C). Read performed with 2μs pulses, cycling performed with 100ns pulses (5MHz).

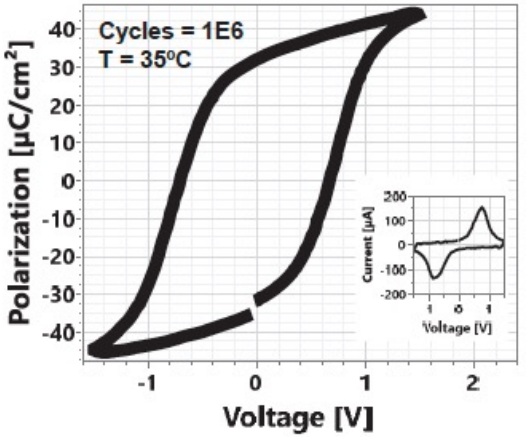


Figure 10. Polarization versus voltage (PV) and corresponding current versus voltage (IV) measured at 35°C after 10^6 cycles.

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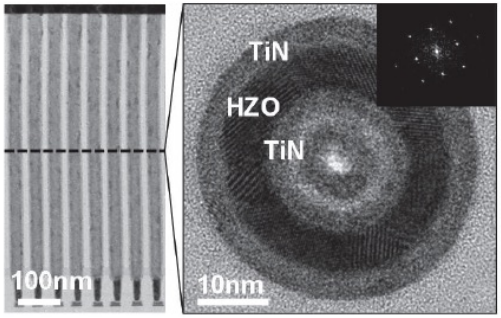

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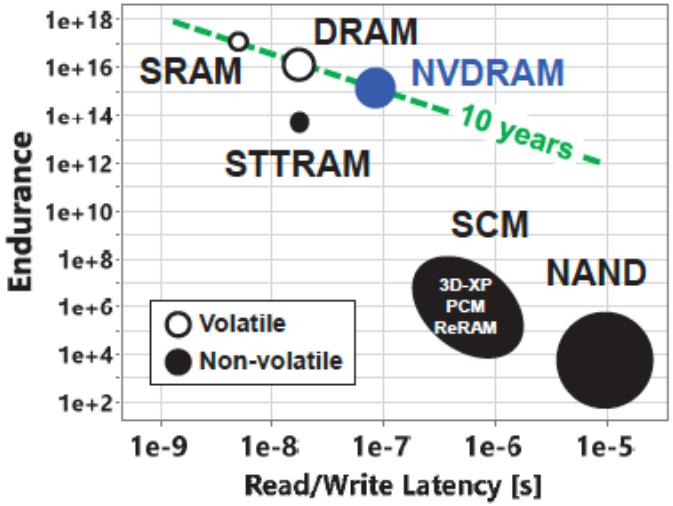
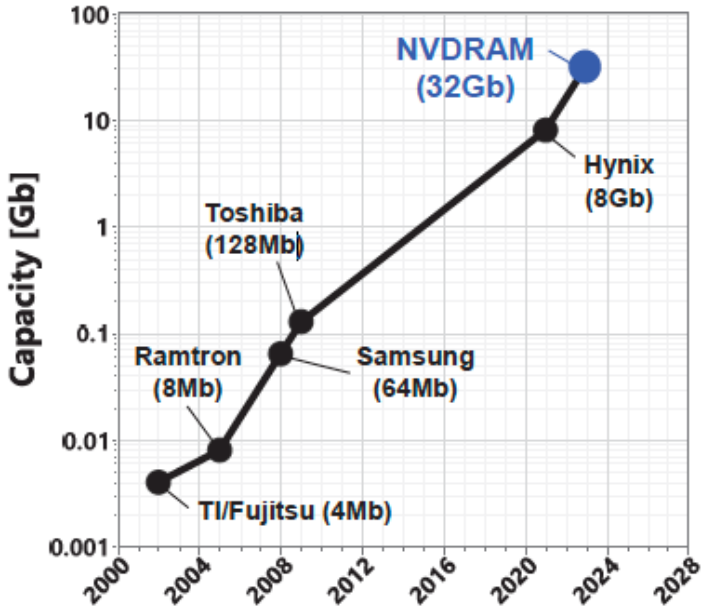


Figure 3. Cycling endurance versus latency. NVDRAM achieves near-DRAM latency and has sufficient cycling endurance to support 10yr product lifetime.



Emerging memories: summary (other companies may show different numbers)

Characteristics of emerging memories validated by the industry (ST Microelectronics assessment, situation for 2022)

	FLASH	MRAM	PCM	RRAM	FeRAM	FeFET
Programming power	~200pJ/bit	~20pJ/bit Exp demo 0.3pJ/bit	~300pJ/bit Exp demo 0.3pJ/bit	~100pJ/bit	~10fJ/bit	~10fJ/bit
Write speed	20µs	20ns Can be 1-10 ns	10-100ns	10-100ns	15ns @ 2.5V	<1µs
Endurance	10^5-10^6	10^6-10^{15}	10^7-10^8	10^5-10^7	>10^{11}	10^5-10^6
Retention	>125°C	85-215°C	165°	>125°	85°C	125°C ??
Extra masks	Very high >10	Limited (3-5)	Limited (3-5)	low (2)	low (2)	low (2)
Bias Usage (HV)	High	low	medium	low	low	low
Process flow	Complex	medium	medium	simple	simple	simple
Scalability	bad	medium	high	high	Poor (2D) High (3D)	high

Conclusions

- There are plenty of new materials, however it is difficult to satisfy memory requirements
- For the moment there is no “single universal memory”
- Technology choice is application-driven
- eNVM is becoming a standard CMOS option
- The focus shifts from “replacing DRAM” to compute-centric memory architectures
- Compute-centric applications (neuromorphic computing, in-memory computing)
- New read/write endurance characteristics enable new circuit design

Key candidates beyond DRAM and FLASH:
Phase Change Memory, Resistive RAM, STTRAM, Ferroelectric RAM